VARIATION-AWARE AND PROCESS-SENSITIVE RELIABILITY SIMULATOR AND ITS APPLICATION FOR ANALOG AND DIGITAL CIRCUITS

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VARIATION-AWARE AND PROCESS-SENSITIVE RELIABILITY SIMULATOR AND ITS APPLICATION FOR ANALOG AND DIGITAL CIRCUITS

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There is nothing either good or bad but thinking makes it so

William Shakespeare

For my parents, Yao Yang and Ying Zhang, who taught me to work hard and dream big,
and who made all of this possible through their love, encouragement and sacrifices

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LIST OF SYMBOLS AND ABBREVIATIONS

BEoL	Back-End-of-Line
BTDDB	Back-End-of-Line Time Dependent Dielectric Breakdown
BTI	Bias Temperature Instability
CA	Contact
CAD	Computer-Aided Design
CMOS	Complementary Metal–Oxide–Semiconductor
DC	Direct Current
EM	Electromigration
FEoL	Front-End-of-Line
FFT	Fast Fourier Transform
FinFET	Fin Field-effect transistor
FPGA	Field-Programmable Gate Array
GOBD	Gate Oxide Time Dependent Dielectric Breakdown
HCI	Hot Carrier Injection
LNA	Low Noise Amplifier
MARS	Multivariate Adaptive Regression Splines
MOL	Middle-of-Line

MTTF	Mean-Time-to-Failure
NBTI	Negative Bias Temperature Instability
NMOS	N-Channel MOSFET
PBTI	Positive Bias Temperature Instability
PC	Polysilicon/high-k Control Gate
PDK	Process Design Kit
PMOS	P-Channel MOSFET
PVT	Process-Voltage-Temperature
RF	Radio Frequency
SIV	Stress-induced-voiding
SPICE	Simulation Program with Integrated Circuit Emphasis
TDDB	Time Dependent Dielectric Breakdown

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SUMMARY

Traditional gate oxide TDDB (GOBD) is one of the main concerns for advanced CMOS technology. The introduction of new device configurations, with smaller feature sizes and thinner oxide thickness, has continuously challenged dielectric breakdown behaviors. With feature size shrinking, the newly emerged middle-of-line (MOL) TDDB has also become a reliability concern for circuit designers.

To help circuit designers design their circuits in a reliable and robust fashion, a reliability simulator for GOBD and MOL TDDB based on vulnerable feature extraction has been developed and implemented. Also, the algorithms to detect and extract vulnerable features for GOBD and MOL TDDB are discussed in detail.

A framework that processing standard cell library, circuit netlist, temperature distribution and activity profile is proposed. Also, the FPGA based activity propagation method to speed up circuit simulation is introduced. The framework also takes different use scenarios into account. By obtaining different operating conditions under use scenarios, the lifetimes of different applications can be assessed.

In addition, process variation is also incorporated in the simulator. The simulator considers the variation in a MOSFET's channel length and gate alignment offset. A CAD-oriented approach is proposed for faster lifetime assessment. The approach pre-characterizes all the standard cells' lifetime with a combination of process variation and input variation. The simulator stores a lookup table for different process variations and input variations for different cells in the library and saves time for recomputing the lifetime for the same cell under different use scenarios.

Moreover, the simulator considers both analog circuit (a receiver system) and digital circuits (ring oscillator, the FFT circuit and the Leon3 microprocessor) to ensure the flexibility of the functionality. The simulator not only considers the lifetime assessment in traditional bulk CMOS technology, but also in the state-of-art FinFET technology.

With the simulator built, one can use it to determine the optimal accelerated life test region for different circuits with respect to different wearout mechanisms. By calculating the lifetimes under different voltages and temperatures for the circuit, the simulator can determine whether a certain wearout mechanism is dominant under certain test conditions and gives the corresponding estimating errors due to sampling and selectivity.

Circuit designers always design the circuit and check for reliability afterwards. The two step process is time-consuming and sometimes the design only meets one of the criteria. The simulator can also be used for analog circuit optimization for optimal performance, power and lifetime in one step. By utilizing Monte Carlo simulation, the simulator obtains various sets of training data on performance, power and lifetime to build the regression model through MARS (multivariate adaptive regression splines). After setting the constraints for different metrics, the simulator will output the optimal design strategies for the input circuit.

CHAPTER 1

INTRODUCTION

The semiconductor industry lives and dies by a simple creed: smaller, faster and cheaper. Manufacturers would like their products to be tiny, since more transistors can be packed onto the same chip. The more the transistors on a single chip, the faster it can operate.

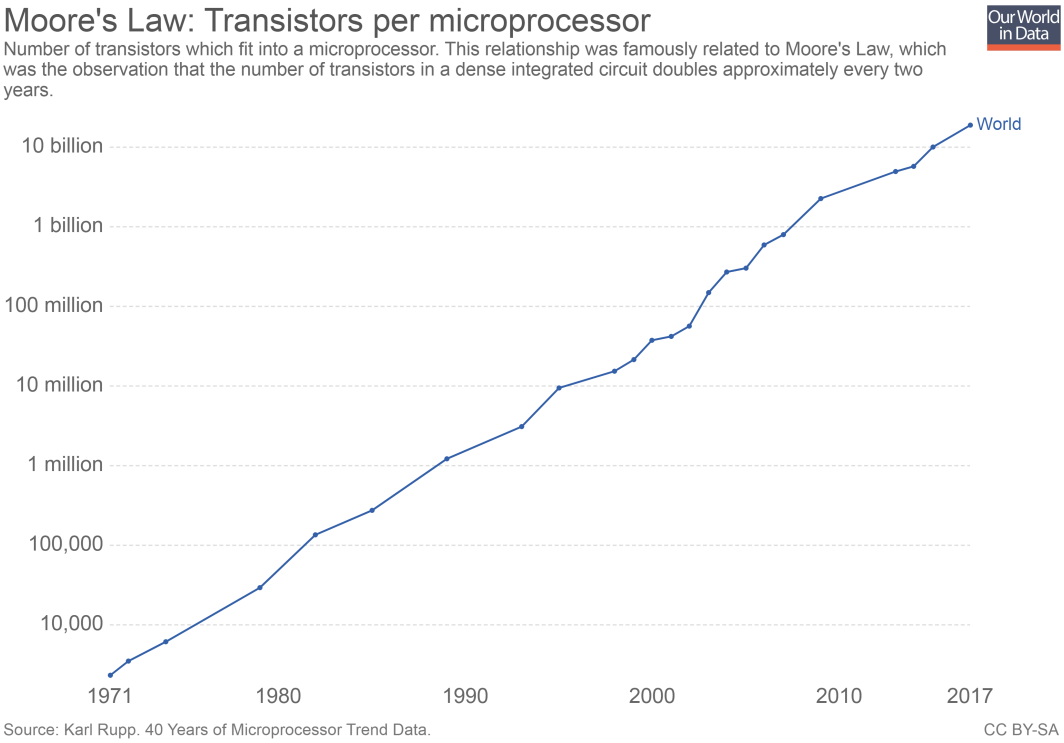


Figure 1.1: Moore's Law: Transistors per microprocessor[1].

In 1965, Gordon Moore noticed that the number of the transistor per square inch on integrated circuits had doubled every year since their invention. He predicted this trend will continue into the foreseeable future. Although the recent pace has slowed for Moore's Law, the doubling of installed transistors on silicon chips occurs closer to every 18 months instead. The 18-month mark is now used as the current definition of Moore's Law, as shown

[1]Source: Karl Rupp. 40 Years of Microprocessor Trend Data.

in Fig. 1.1.

As we are trying to keep up with the Moore's Law, the oxide thickness of a transistor has become thinner than ever and the layout is made as compact as possible, leading to a series of reliability issues in device reliability.

1.1 Motivation

GOBD is one of the main concerns for advanced CMOS technology, the introduction of new device configurations, such as smaller feature sizes and thinner oxide thicknesses, has continuously challenged dielectric breakdown behavior. Gate oxide TDDB (GOBD) happens when a breakdown path forms in the gate oxide, causing a punchthrough from gate to channel which results the inability to control the current flow of the transistor and largely decreases gate input resistance. A new source of dielectric breakdown is call Middle-of-Line (MOL) TDDB, which is the breakdown between the polysilicon/high-k control gate (PC) and diffusion contacts (CA) [1–9]. This type of breakdown happens when there is a conductive path formed between a PC and CA pair, leading to a functional failure of the victim transistor. The illustration of GOBD and MOL TDDB of a bulk CMOS transistor is shown in Fig. 1.2.

1.1.1 Newly Emerged MOL TDDB Reliability Concern in Circuits

Evaluating the reliability of modern electronic components is an involved and costly problem, exacerbated by continual improvements in failure rates and by continual changes in technology. In the case of integrated circuits there is the additional problem of the inherent functional complexity of the basic element. All of these imply significantly higher costs for life-testing and circuit design [10].

Although lots of researches have been done on the topic of device TDDB, only a few works have addressed GOBD at the circuit-level [11–13] and none of them consider MOL TDDB in circuits. As the feature size become smaller, the dielectrics between gate and

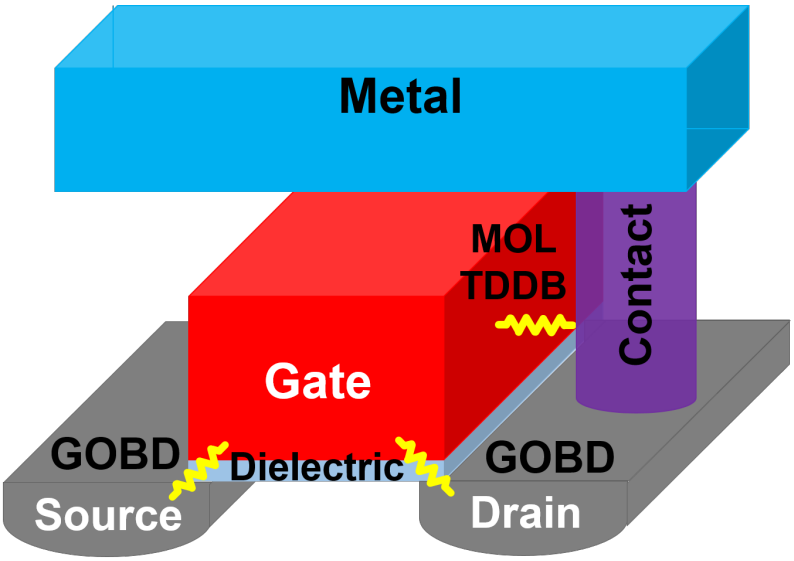


Figure 1.2: Illustration of GOBD and MOL TDDB in a bulk CMOS transistor

contacts are more vulnerable than ever and need to be carefully considered for reliability assessment.

1.1.2 Reliability Concerns in Traditional Bulk CMOS Technology and FinFET Technology

Since assessment of MOL TDDB involves detailed analysis of a standard cell layout, it is a technology-dependent process. Every technology has its own layout rules and specific interconnect; to cope with different technologies, detailed analysis for each layer and every interconnect is needed.

Lots of commercial tools have added reliability assessment for FinFET technology, however, the detailed algorithms and flows are usually not available to the public. This makes it difficult for researchers who would like to investigate reliability concerns at the circuit-level.

1.1.3 Optimal Accelerated Life Test

Accelerated life tests (tests at high voltages and temperatures) are often applied to stress CMOS circuits to assess their lifetimes. Device level degradation models enable the pos-

sibility to test at accelerated conditions and to predict the circuit's lifetime at normal operating conditions. More importantly, accelerated tests can be used to tell which wearout mechanism is dominant in a target circuit; and circuit designers can use such information to improve and redesign their circuits for robust operations and a longer lifetime.

Device-level degradation models act as a link from transistor to circuit-level lifetime results; and thus, the more accurate the parameters of device-level models are, the more accurate the final lifetime prediction result will be. To obtain accurate model parameters, we need to decouple different wearout mechanisms while testing, i.e., to test at certain conditions where only one wearout mechanism is dominant.

If researchers have a simulator to get information about which region is better for testing, a lot of effort and time can be saved, and more accurate results will be collected for building wearout models.

1.1.4 Circuit Lifetime Optimization

Computer-aided circuit optimization is certainly one of the most active areas of interest, since the size of circuits grows exponentially. Advances have been made in several major directions. The development of large-scale network simulation and optimization techniques have been motivated by the requirements of the VLSI era. Optimization methods have evolved from simple, low-dimension-oriented algorithms into sophisticated and powerful ones[14].

Although the optimization methods have evolved, circuit designers still design the circuit for performance and check for reliability afterwards. The two-step process is time-consuming and usually causes delay in delivering of a new product. Thus, a one-step performance, power, lifetime sensitive optimization framework is needed for faster circuit design.

1.2 Research Objective and Contribution

This thesis focuses on understanding the details and challenges discussed above, and developing a TDDB lifetime simulator for both analog and digital circuits. This work consists of four key topics summarized as follows.

1. **Compact wearout models and vulnerable feature extraction.** First, the compact device models for GOBD and MOL TDDB are introduced. The models act as a link between device-level wearout to circuit-level wearout. Next, the widely used Weibull distribution is utilized in the simulator to characterize lifetime of each transistor/vulnerable feature in the circuit. Also, the variation modeling is introduced. The corresponding vulnerable feature extraction algorithms is proposed and discussed in detail.

2. **Lifetime assessment flow.** The lifetime assessment flow for circuits is presented. The extraction of circuit operating conditions, including temperature, stress probability, is discussed. Also, the CAD-oriented standard cell library characterization method, which considers process variation and input variation is introduced. The speed of our simulator is discussed. The lifetimes under different use scenarios are also presented. The simulator is also able to extract the most vulnerable feature in a standard cell layout.

3. **Parameter extraction for wearout models.** To find the optimal test region for wearout model parameter estimation, we first use the lifetime simulator to find the selectivity of the target wearout mechanism. Then, with the selectivity, the estimation from selectivity can be obtained, and combined with the error from sampling, we can find the optimal test region for minimum errors.

4. **Framework for analog circuit lifetime optimization.** An optimization framework that consider circuit's performance, power and lifetime is proposed. MARS is used

as our regression tools to connect circuit design parameters to circuit's performance metrics and lifetime. By utilizing the MARS model, the optimization framework is able to consider performance metrics and lifetime in an one-step process, saving the traditional turnaround time to design first and check reliability later. Multiple optimization modes are provided for the designer, circuit designers can choose the specific one depending on their needs and applications.

1.3 Organization of the Thesis

The rest of the thesis is organized as follow.

In chapter 2, previous studies on device and circuit reliability are discussed. Also, the need for considering process variation is stated. In addition, the effort made by other researchers for circuit optimization is introduced.

In chapter 3, device-level wearout models for GOBD and MOL TDDB are introduced. The methodology to model variability in circuits is also discussed. In addition, the algorithms for vulnerable feature extraction are presented and discussed in detail.

In chapter 4, the lifetime assessment flow for circuits is presented. Extraction of circuit operating conditions is discussed. The characterization of standard cell lifetime is presented in detail. Also, the full chip lifetime analysis incorporating process, voltage and temperature variation is studied.

In chapter 5, the methodology to accurately estimate circuit lifetime parameters is proposed. The applications in analog and digital circuits across different technologies are also presented.

In chapter 6, a FEoL TDDB lifetime and power sensitive design framework to help designers to assess the impact of design parameters, such as transistor width and length is built. A receiver is taken as an example to illustrate the functionality of our framework. By utilizing Monte Carlo simulation, our predictive model is built through MARS. With the built-up model, we can generate our candidate solutions in the model space and use

predefined constraints to find our optimal design strategy.

This thesis is summarized in chapter 7 and the discussion of potential future work is presented.

CHAPTER 2
RELIABILITY ANALYSIS FOR MODERN BULK CMOS AND FINFET TECHNOLOGIES

In the past few decades, researchers have mainly focused on device-level reliability studies. There are three main type of Front End of Line (FEoL) wearout mechanisms, that is, gate oxide breakdown (GOBD) [15–19], hot carrier injection (HCI) [20–24], bias temperature instability (BTI) [25–30]. For Back End of Line (BEoL) wearout mechanisms, there are BEoL time-dependent dielectric breakdown (BTDDB) [31–36] electromigration (EM) [37–44] and stress-induced voiding (SIV) [45–51]. Also, there is the newly emerged middle-of-line time-dependent dielectric breakdown (MOL TDDB) [2, 9, 52]. Recent studies have assessed the reliability concern in circuit-level. In this chapter, reliability studies on circuit-level are explored and summarized.

2.1 Circuit-Level TDDB Assessment

A continuous increase in the transistor' density in a single die accompanied by the reduction of gate oxide thickness makes TDDB assessment more important than ever. With the aggressive technology scaling, the impact of process variation becomes an inevitable concern. Robust circuit design depends on a more complete characterization of these variations and their impact on reliability assessment. The variations in a transistor's length and the gate location offset have a significant impact on TDDB lifetime; and thus, we need to take it into consideration when building a lifetime simulator.

There are studies of MOL TDDB on dielectric materials [2, 4]; also, in previous circuit-level reliability studies, researchers have investigated BTI [11, 53–61], HCI [11, 55–57, 62, 63], GOBD [11–13, 64–69], BTDDB [70–74], EM [75, 76], SIV [77]. Also, there are some studies about fault detection [78, 79]. However, no study has been conducted to investigate

MOL TDDB's effect on circuits and microprocessors.

2.2 Process Variation

Moore's Law driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As advanced technologies continue the pursuit of Moore's Law, one of the most significant challenges is management of variation. The continued decrease in the ratio of feature sizes to fundamental dimensions means that management of variation will become an increasingly important issue in further technology scaling [80]. Process variation has a significant impact in lifetime assessment. The variation in a transistor's gate length adds uncertainty in both FEOL and MOL TDDB lifetime. In addition, the mismatch in gate location makes the linespace decrease on one side, which increases the electric field in the adjacent PA-CA pair.

With the aggressive technology scaling, the impact of process variation becomes an inevitable concern. Robust circuit design depends on a more complete characterization of these variations and their impact on reliability assessment; and thus, we need to take them into consideration when building a lifetime simulator. To avoid overoptimistic prediction for circuit lifetime, our lifetime simulator needs to incorporate the process variation when analyzing the circuit. We use Monte Carlo simulation on the circuit to generate samples to consider the process variations and to obtain the worst corner case.

2.3 Wearout Model Parameter Estimation

To guarantee reliable operations of circuits and systems, semiconductor devices are tested with accelerated life tests to estimate device-level reliability and to develop a predictive reliability model for circuits and systems based on the estimated reliability of devices. Nevertheless, to accurately estimate the lifetime of a system, reliability testing at the system level is necessary [81].

Accelerated life tests (tests at high voltages and temperatures) are often applied to stress

CMOS circuits to assess their lifetimes. Device level degradation models enable the possibility to test at accelerated conditions and to predict the circuit's lifetime at normal operating conditions. More importantly, accelerated tests can be used to tell which wearout mechanism is dominant in a target circuit; and circuit designers can use such information to improve and redesign their circuits for robust operation and a longer lifetime.

To achieve this goal, we must first identify the lifetime-limiting mechanisms in the circuit; and we need to find the optimal test conditions for each of these wearout mechanisms. That is, we would like to test the circuit with test conditions where only one wearout mechanism is likely to happen. Our reliability simulator is capable of this task as well. To find optimal test region for both analog and digital circuits, different methodologies should be implemented since we need different flow to extract the stress profile in analog and digital circuits.

2.4 Performance Improvement and Lifetime Enhancement

Lots of works have been done to optimize circuit performance, both in digital and analog circuits. For digital circuit, most of them are focused on the area, power and timing tradeoff [82–84]; as for the analog counterpart, a symbolic simulation method is proposed for optimization [85], and process variation is taken into consideration [86]. However, none of them have considered circuit reliability when performing optimization. We must take wearout mechanisms as a significant factor when designing in modern bulk CMOS and FinFET technologies.

For analog circuits, our focus is tuning the size of each transistor; and thus, we use multivariate adaptive regression splines (MARS) as our regression method to build a high dimensional model, which considers lifetime, power and performance as a function of size. In this way, we can find the optimal solution in the candidate space.

2.5 Summary

The objective of this study is threefold. First, we propose a methodology and its corresponding algorithms to extract vulnerable features for GOBD and MOL TDDB for both bulk CMOS and FinFET technology. The layout of FinFET technology varies significantly compared to traditional bulk CMOS technology and we need to implement different algorithms to extract the corresponding vulnerable features. In traditional bulk CMOS technology, there is only one type of vulnerable feature; whereas for FinFET technology, multiple possible vulnerable features may exist. A netlist-oriented GOBD TDDB analysis method and a standard-cell based MOL TDDB analysis flow are discussed in detail. Combined with vulnerable features, the circuits' activity profile and temperature map are used for lifetime calculation of the circuit. Second, we incorporate process variation into our lifetime simulator and analyze its impact on circuit lifetime; Monte-Carlo simulation is utilized. To demonstrate our simulator's functionality, we take an 8-bit FFT circuit and a state-of-art Leon3 microprocessor as example to assess their lifetime under TDDB. For Leon3, we also consider the impact of use scenarios on the lifetime. Third, we use our simulator to find the optimal test region for accelerated life test in both analog and digital circuits for different wearout mechanisms; in addition, we develop an optimization framework for a circuit considering circuit lifetime in the design phase.

CHAPTER 3
COMPACT WEAROUT MODELS AND VULNERABLE FEATURE EXTRACTION

In this chapter, device-level wearout models for GOBD and MOL TDDB are introduced. The methodology to model variability in circuits is also discussed. In addition, the algorithms for vulnerable feature extraction are presented. The related publications can be found in [87–91]

3.1 Device-Level Wearout Models

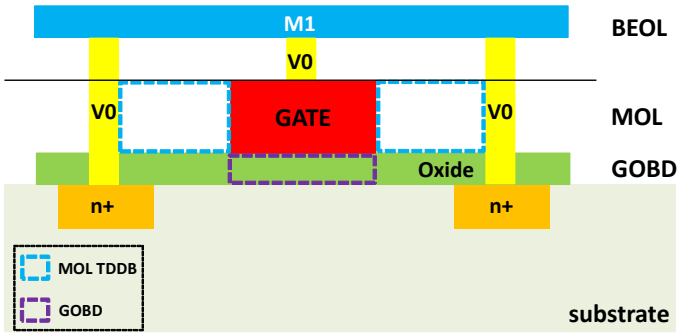
Fig. 3.1 shows the breakdown paths of GOBD and MOL TDDB. GOBD is the breakdown between the gate and substrate; whereas MOL TDDB is the breakdown between the gate and its adjacent contact or active interconnect layer.

3.1.1 GOBD

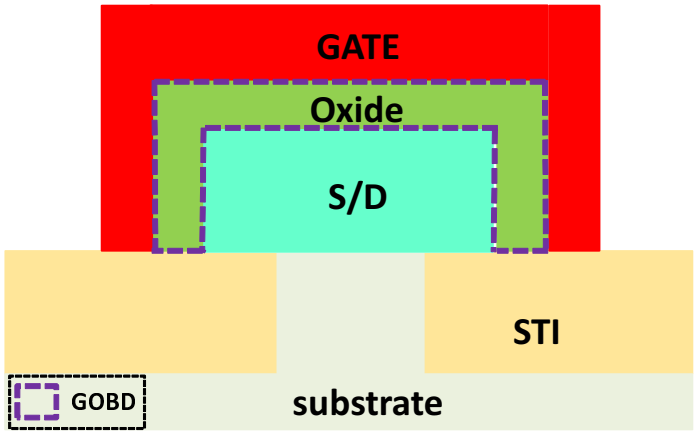
GOBD is described as the build-up of traps in the gate oxide as a function of time under voltage and thermal stress. We use the hard breakdown (HBD) model to characterize the transistor lifetime distribution. For ultra-thin (<5nm) gate dielectrics, the time-to-failure due to gate-oxide degradation can be derived by connecting the oxide degradation model to the Weibull failure distribution function [74] which is described by a shape parameter, β and a characteristic lifetime η, which is the time-to-failure at the 63% probability point, i.e.,

$$\eta = A_{ox}(\frac{1}{WL})^{\frac{1}{\beta}} e^{-\frac{1}{\beta}} V^{a+bT} exp(\frac{c}{T} + \frac{d}{T^2}) s^{-1} \tag{3.1}$$

where *W* and *L* are the device width and length, respectively, *s* is the probability of stress,



(a)



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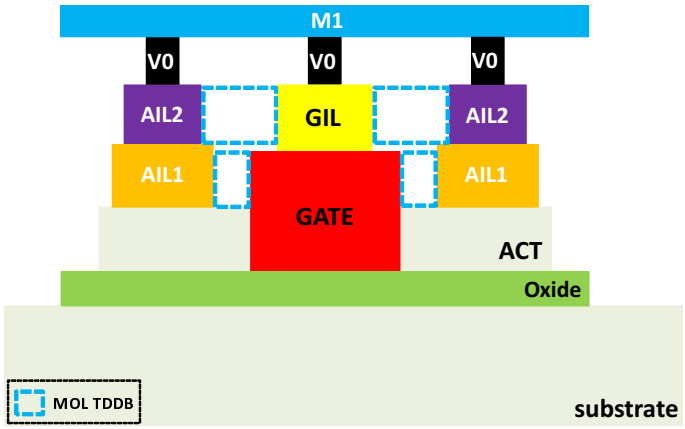


(c)

Figure 3.1: Illustration of (a) gate oxide and MOL TDDB in traditional bulk CMOS and (b) MOL TDDB and (c) gate oxide TDDB in FinFET CMOS. The location of GOBD is indicated by the dashed purple box and the location of MOS TDDB is indicated by the dashed blue boxes.

Table 3.1: Parameters Used for GOBD

A_{ox}	β	*a*	*b*	*c*	*d*
5e7	1.64	-78	0.081	8.81e3	-7.75e5

Table 3.2: Parameters Used for MOL TDDB

A_{MTDDB}	β	γ(cm/MV)	*m*	E_a(eV)
6.76e-4	0.98	8.723113	1	0.5

T is temperature, *V* is gate voltage, and *a*, *b*, *c*, *d*, and A_{ox} are fitting parameters. To obtain those parameters, p+poly/n-Si capacitors are used as the test structure and tested under various voltages and temperatures [92]. The detailed values used in this work are shown in Table 3.1.

3.1.2 MOL TDDB

Although Back-End-of-Line (BEOL) TDDB is not discussed in this paper, the device-level lifetime model for MOL TDDB is similar to that of BEOL TDDB [93] as follows:

$$\eta = A_{MTDDB} {L_i}^{-\frac{1}{\beta_i}} exp(-\gamma E^m + \frac{E_a}{kT}) \tag{3.2}$$

where A_{MTDDB} is a constant that depends on the material properties of the dielectric, $\gamma$is the field acceleration factor, and E_a is the activation energy (0.5eV), L_i is the vulnerable length, and *m* is 1 for E model. The temperature dependence is modelled with the Arrhenius relationship [94], where *k* is the Boltzmann constant.

To test MOL PC-CA lifetime, SiN and low-k films were used between the gates and contacts as the insulation spacer film. The test structure consists of a MOS capacitor electrode and the adjacent contact. MOL structures were laid on shallow trench isolation (STI) oxide to isolate the PC-CA breakdown from the gate dielectric breakdown. All parameters are extracted from results in [3]. The parameters used in this work are shown in Table 3.2. Other papers [1, 2, 4–9] indicate the importance of MOL TDDB, but provide no numerical

data. Because this work is based on limited experimental data, the results must be interpreted as indicative of trends as a function of technology scaling, while identification of the limiting wearout mechanism for each technology generation would require additional experimental data. Limiting cells can be identified, since cells are compared with the same model parameters.

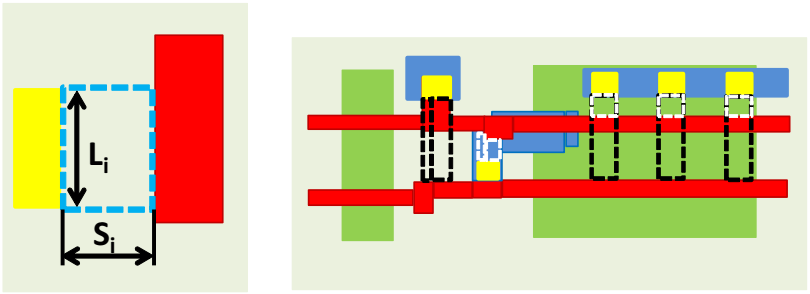


Figure 3.2: MOL TDDB vulnerable features: illustration of linespace Si and vulnerable length Li and vulnerable features in a layout.

The MOL TDDB features are shown in Fig. 3.2, where L_i and S_i are indicated. The yellow square represents a contact, the honeydew color stands for the dielectric, while the red rectangle stands for one poly segment. The dashed boxes are potential vulnerable features.

3.2 Variation Modeling

In this study, we consider process variation's impact on circuit lifetime. Table 3.3 presents the process variation parameters, where ΔLn and ΔLp denote channel length in NMOS and PMOS devices separately, ΔLo denotes the offset in gate location. All the variations considered are intra-die variation. In MOL TDDB, the channel length variation will cause the linespace to increase or decrease in the same direction, while the gate location offset will increase the linespace on one side and decrease it on the other side, as shown in Fig. 3.3. The situation without gate length and location offset is shown in Fig. 3.3(a). Fig. 3.3(b) shows the case where gate length varies, causing the linespace on both sides to decrease, while Fig. 3.3(c) presents the gate location shift, making the linespace on one side to in-

Table 3.3: Variation and Corners

Variation	Random Variations	Corners
ΔL_n	Gaussian, $3\sigma = 20\%$	$[-30\%, 30\%]$
ΔL_p	Gaussian, $3\sigma = 20\%$	$[-30\%, 30\%]$
ΔL_o	Gaussian, $3\sigma = 20\%$	$[-30\%, 30\%]$

crease and on the other side to decrease.

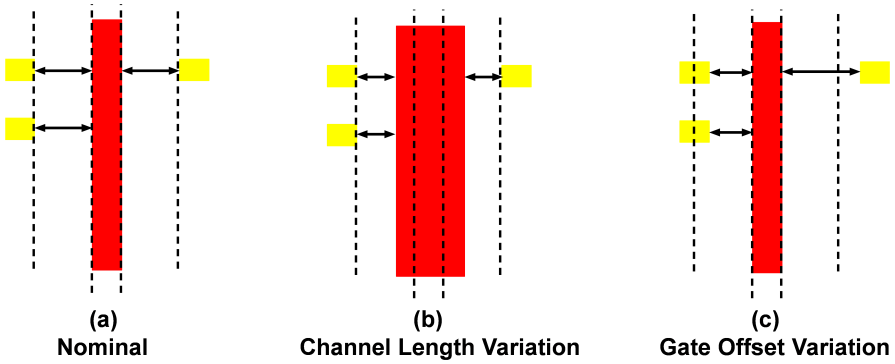


Figure 3.3: Process variations' impact on vulnerable feature: (a) normal (b) gate length variation (c) gate location offset

3.3 Circuit Lifetime Calculation

To combine different device lifetimes in a standard cell, we assume a standard cell is composed of n devices (n vulnerable features for MOL TDDB), each modelled with a Weibull distribution, for each wearout mechanism. The characteristic lifetime of the cell, η_{cell}, is a combination of Weibull distributions and is the solution of [70–72],

$$1 = \sum_{i=1}^{n} (\eta_{cell}/\eta_i)^{\beta_i} \tag{3.3}$$

where $\eta_i, i = 1, ..., n$ are the characteristic lifetimes of all of the devices; and $\beta_i, i = 1, ..., n$ are the corresponding shape parameters. Similarly [71],

$$\beta_{cell} = \sum_{i=1}^{n} \beta_i (\eta_{cell}/\eta_i)^{\beta_i} \tag{3.4}$$

If the shape parameter is the same for each device (feature), which is typically assumed,

$$\eta_{cell} = (\sum_{i=1}^{n} \eta_i^{-\beta})^{-1/\beta} \tag{3.5}$$

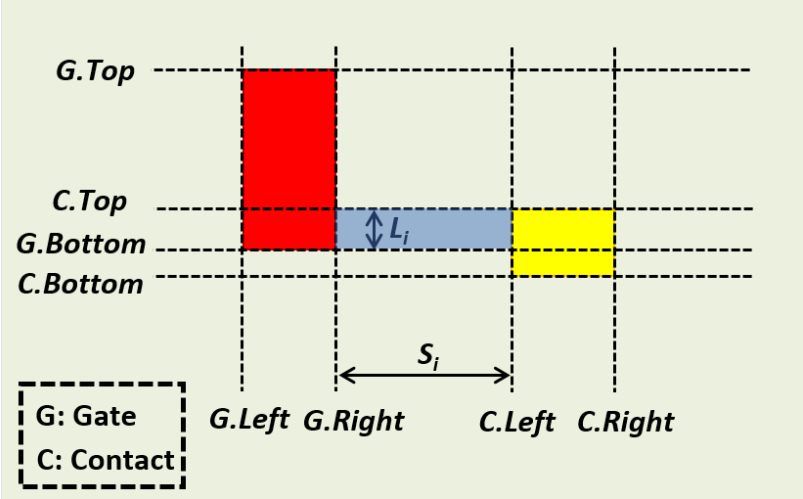


Figure 3.4: MOL TDDB vulnerable feature detail illustration.

To calculate the FEOL TDDB lifetime of a standard cell, we need to obtain the gate-source voltage, V_{gs}, for each transistor and analyze each transistor's gate stress probability p. As for MOL TDDB, we should analyze the standard cell's layout. For each adjacent PC-CA pair, we need to extract the linespace S_i and vulnerable length L_i, as shown in Fig. 3.4. After that, for each PC-CA pair, the vulnerable feature pair (S_i, L_i) is associated with the poly-contact voltage difference V. The stress probability of a single dielectric segment feature is calculated as follows:

$$p_{total} = p_1(1 - p_2) + p_2(1 - p_1) \tag{3.6}$$

where p_1 and p_2 are the probabilities of the poly and contact being at logic "1", respectively.

To calculate the probability of failure at time t for each circuit, we use the Weibull distribution, with characteristic lifetime, η, and shape parameter, β. The probability of

failure at time t is calculated with the following equation [73]:

$$P(t) = 1 - exp(-(\frac{t}{\eta})^{\beta}) \tag{3.7}$$

3.4 TDDB Vulnerable Feature Extraction

In this section, we will introduce the algorithms to extract vulnerable features for both GOBD and MOL TDDB. Since the device-level wearout models for GOBD and MOL TDDB are different, the algorithm for each is also unique. In addition, we need to develop algorithms corresponding to bulk CMOS and FinFET separately.

3.4.1 GOBD Vulnerable Feature Extraction

To characterize device lifetime under GOBD, we need to extract the device width (W) and channel length (L). By inspecting the netlist of the standard cell, we can get W and L for each transistor.

As for transistor in FinFET technology, instead of using the width (W) directly from the netlist, which represents the drawn width of the source and drain, we should calculate the effective width [95] as follows,

$$W_{eff} = T_{fin} + 2H_{fin} \tag{3.8}$$

where T_{fin} is the fin thickness and H_fin is the fin height.

In addition, we need to take the number of fins into account, the total effective width is obtained by,

$$W_{eff,total} = n_{fin} \cdot W_{eff} \tag{3.9}$$

where n_{fin} is the number of fins in the transistor.

For each standard cell in the technology library, we perform the same process and store the information in a Python dictionary for later use.

3.4.2 MOL TDDB Vulnerable Feature Extraction in Bulk CMOS Technology

To extract the vulnerable features for MOL TDDB, our simulator needs to be able to analyze the layout. As shown in Fig. 3.2, we only need to focus on the vulnerable feature between adjacent contacts and poly segments, which are shown as dashed white squares. We should ignore the vulnerable features between a contact and the more distant poly segments, which are shown in dashed black squares, since those features are separated by the poly segments in the middle and the electric fields will be shielded. Notice that the metal is represented as a blue rectangle, the green rectangle is the active implant area, the poly gate is represented by separate red rectangles in the layout.

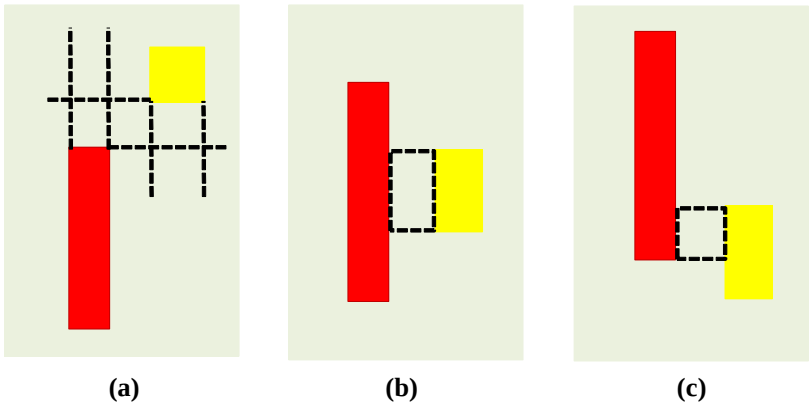


Figure 3.5: Vulnerable feature categories.

Fig. 3.5 summarizes the categories of vulnerable features that can appear in a layout. As we can see in Fig. 3.5(a), when there is no overlap between a PC-CA pair; we call this the "nonoverlap" case (no vulnerable feature exists). As in Fig. 3.5(b) and (c), when there are vulnerable features, we call this the "overlap" relationship. Fig. 3.5(b) and (c) are the full "overlap" and partial "overlap" situations, respectively.

A vulnerable feature only exists in the "overlap" situation, and thus, our algorithm detects this situation. In the layout file, the electrical net connection is stored as a single

Algorithm 1: find poly segments connected to pin

```
Input: standard cell layout information (.lef file)
Output: poly connection information of each pin in each
standard cell
for each pin in standard cell:
   find the poly segements (poly_initial) that are
connected to the pin (contact)
   create one queue and one list
      // queue: store poly segements wait to be processed
      // list: store poly segments that is connected to the
pin
   queue.push(poly_initial)
   while queue.empty() is False:
         item = queue.pop()
         if item not in list:
            find poly segements that are adjacent to item,
            store them in queue
            list.append(item)
         end
   end
end
#store the result in a dictionary: std_cell_poly_info
```

Figure 3.6: Algorithm for finding connected poly segments.

point coordinate (x, y), while a rectangle is stored as its vertices' coordinates: bottom left corner (Left, Bottom), and the upper right corner (Right, Top), shown in Fig. 3.4.

We start by extracting the poly features connected to a single net. Since we would like to associate gate stress with connected poly segments, we need to collect all the poly segments connected to one net together. We start by finding the top layer to which the net is directly connected and continue the process downward in the stack. In a standard cell, in most cases, the top layer will be a metal layer ($M1$ or $M2$) depending on the type of cell being analyzed.

The algorithm is shown in Fig. 3.6. We utilize a queue and a list in the algorithm; at the beginning, we push the poly segments under the contact net into the processing queue;

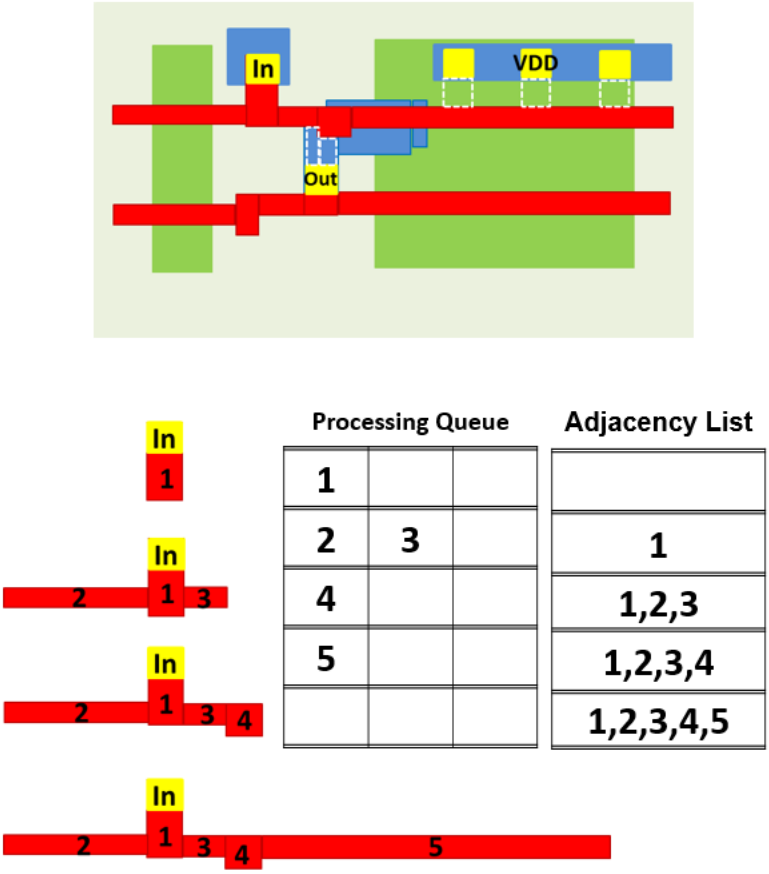


Figure 3.7: Detail explanation of algorithm 1.

then we pop one element from the processing queue and check whether an adjacent poly segment exists. If such a poly segment exists and is not in the result list, we push this poly segment into our queue (for the later adjacency check). In the meantime, we append the popped element to our result list, which stores all the poly segments connected to the target net. This process ends when the queue is empty, and we have determined all the poly segments connected to the net in the result list. We store the extracted information in the *std_cell_poly_info* dictionary.

For a detail explanation for algorithm 1, we use Fig. 3.7 to illustrate how the algorithm works. Suppose we are extracting all the connection to the input pin ”in”; we first find the segment that the pin is directly connected to (segment 1) and add it to the processing queue, . Then we perform breadth-first-search for segment 1, to find all the adjacent connections

Algorithm 2: vulnerable feature extraction

```
Input: standard cell layout information (.txt file)
Output: vulnerable feature for each standard cell
for each pin in standard cell:
   for each pin in std_cell_info[pin']     (pin != pin'):
      if max(G.Bottom, C.Bottom) < min(G.Top, C.Top):
         Li = min(G.Top, C.Top) - max(G.Bottom, C.Bottom)
         X_coord = sort([G.Left, G.Right, C.Left, C.Right])
         Si = X_coord[2] - X_coord[1]
      end
   end
end
#std_cell_info is a dictionrary which stores each pin
connected layers
```

Figure 3.8: Vulnerable feature extraction.

of segment 1 and we add segment 1 into the adjacency list. Thus, in the processing queue, we now have segment 2 and 3, and adjacency list, we have segment 1. We repeat the process, and add segment 4 into the processing queue, and add 2 and 3 to the adjacency list (we do not add what is already in the adjacency list back to the processing queue). If the processing queue is empty, we find all the connection to the pin we processed.

With the poly segment connection information available, we can extract the vulnerable features in the standard cell layout. In Fig. 3.8, the vulnerable feature extraction algorithm is presented. Since a vulnerable feature only exists in the "overlap" configuration of a PC-CA pair, we need to determine whether a poly segment and a contact are indeed in the "overlap" configuration. To achieve this, we focus on the vertical coordinates of the rectangle. If a PC-CA pair "overlap", the maximum y value of the bottom left corner of the PC and CA, max(*G.Bottom*, *C.Bottom*) must be less than the minimum y value of the upper right corner of PC and CA, min(*G.Top*, *C.Top*).

If the vulnerable feature does exist, we perform the feature extraction step. The vulner-

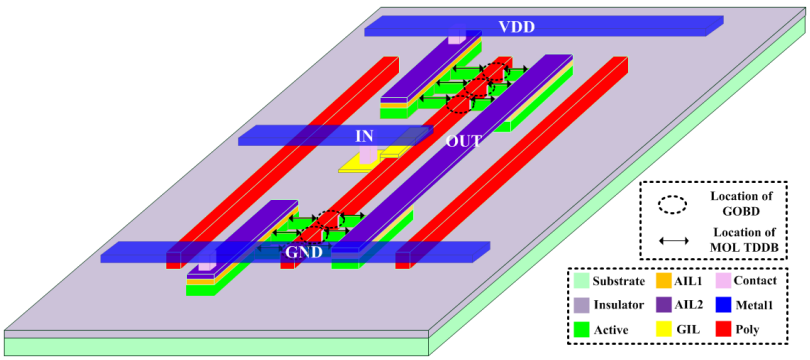


Figure 3.9: 3D inverter view of MOL TDDB and GOBD in FinFET.

able length L_i is computed as follows,

$$L_i = min(G.Top, C.Top) - max(G.Bottom, C.Bottom) \tag{3.10}$$

To extract the linespace S_i between the PC-CA pair, we need to sort the horizontal coordinates and put them into an array $X_{coord}[]$ first. After sorting, the linespace can be obtained by the subtraction of the middle two elements,

$$S_i = X_{coord}[2] - X_{coord}[1] \tag{3.11}$$

3.4.3 MOL TDDB Vulnerable Feature Extraction in FinFET Technology

As we can see in Fig. 3.1(b), there are two types of MOL TDDB features; one is the GATE-AIL1 pair and the other is the GIL-AIL2 pair. We need to extract all the existing vulnerable features of these two types.

In Fig. 3.9, L_i and S_i are indicated. The yellow square represents the AIL1 layer; the red square stands for the gate. The blue dashed squares are the vulnerable features and our goal is to extract these vulnerable features in a standard cell layout. Also, we only consider the nearest vulnerable feature as discussed previously.

We implemented the NanGate 15nm Open Cell Library [96] for FinFET technology. To identify the vulnerable features in a standard cell layout, we find the electrical net to which

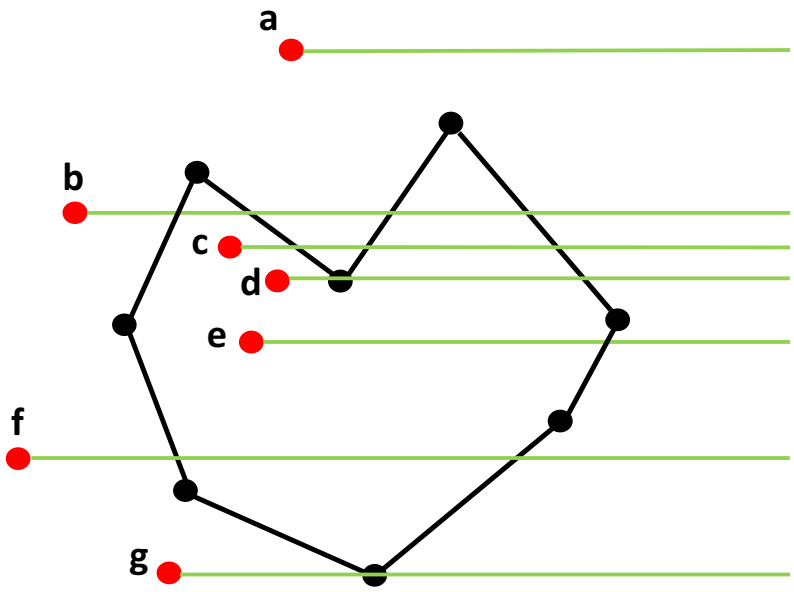


Figure 3.10: Vulnerable feature categories.

the corresponding segment (GATE, AIL1 and AIL2) is connected. This is because when in the later step where the lifetime of vulnerable features is calculated, the stress profile between two segments that are connected to two different nets is needed.

As there are more layers present under a single net, we need a subtler algorithm to determine the net's connection segments. Also, in the FinFET layout file, some layers are drawn as rectangle segments with four vertices, and the others are drawn as polygons which contain more than four vertices. The situation where there are irregular geometries adds complexity to our problem, and we utilize the point inclusion algorithm to determine the direct layer to which a pin is connected.

In our simulator, the ray-casting algorithm [97] has been implemented to find the connected layer. If the number of crossings is odd, the point is inside a polygon. Fig. 3.10 gives a set of example points which we need to test. The Python implementation of the ray-casting algorithm to determine whether a point is inside a polygon is presented in Fig. 3.11

After finding the net's directly connected layer's segment, we start to process downward to find all the layers to which the net is connected. There are two types of vertical

Algorithm 3: point inclusion algorithm

Input: polygon (poly), point (p)
Output: whether the test point is inside the polygon

```
def PinPoly(poly, p):
    nvert = number of vertex in the polygon
    testx = p.x
    testy = p.y
    result = False
    i = 0
    j = nvert - 1
    while ( i < nvert):
      if ( ((poly.Vertex[i].y > testy) != (poly.Vertex[j].y > testy))
     and  (testx < (poly.Vertex[j].x - poly.Vertex[i].x)
     * (testy-poly.Vertex[i].y) / (poly.Vertex[j].y-poly.Vertex[i].y)
     + self.Vertex[i].x)):
         result = !result
      j = i
      i = i + 1
    return result
```

Figure 3.11: Point inclusion algorithm.

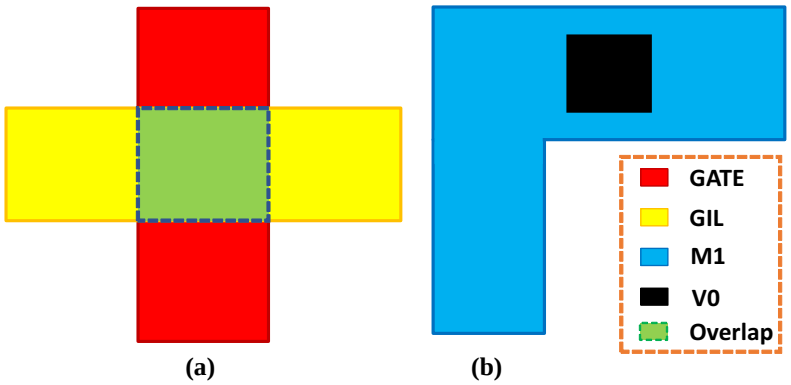


Figure 3.12: Vertical connections.

connection we could find in a standard cell layout, which are illustrated in Fig. 3.12. In Fig. 3.12(a), the vertical connection situation happens between the GIL and GATE layer, while most of the vertical connection situations are presented in Fig. 3.12(b).

The algorithm to find overlap between two rectangles is easy to implement. The detailed implementation can be found in Fig. 3.13. We use contradiction to prove the “if statement”. Any one of the following four cases guarantees that no overlap exists between rectangles

Algorithm 4: rectangle overlap determination

Input: rectangle_A (RectA), rectangle_B (RectB)
Output: whether the two rectangles overlap
if (RectA.Left < RectB.Right and RectA.Right > RectB.Left and
RectA.Top > RectB.Bottom and RectA.Bottom < RectB.Top):
return True
else:
return False
end

Figure 3.13: Vertical connection determination algorithm.

A and B:

Case #1: If A's left edge is to the right of B's right edge (A is totally to the right of B).

Case #2: If A's right edge is to the left of B's left edge (A is totally to the left of B).

Case #3: If A's top edge is below B's bottom edge (A is totally below B).

Case #4: If A's bottom edge is above B's top edge (A is totally above B).

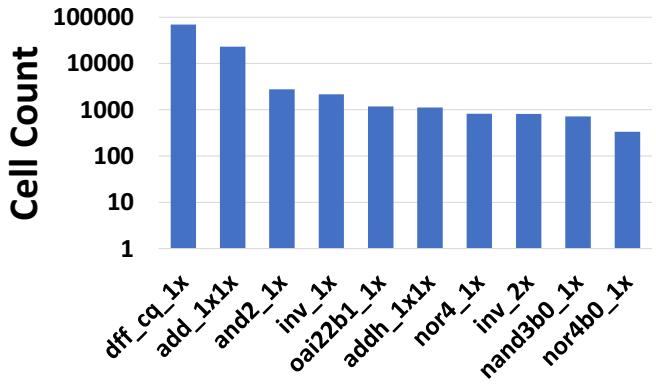
As for the situation in Fig. 3.12(b), we can utilize the point inclusion algorithm. That is, if one of the via's vertices is inside the polygon, then the two are vertically connected. Once the layer connection determination is finished, we store the net's connected layers for each standard cell in a Python dictionary named "*std_cell_info*". With all the information ready, like traditional bulk CMOS case, we use the algorithm in Fig. 3.8 to extract vulnerable features.

CHAPTER 4

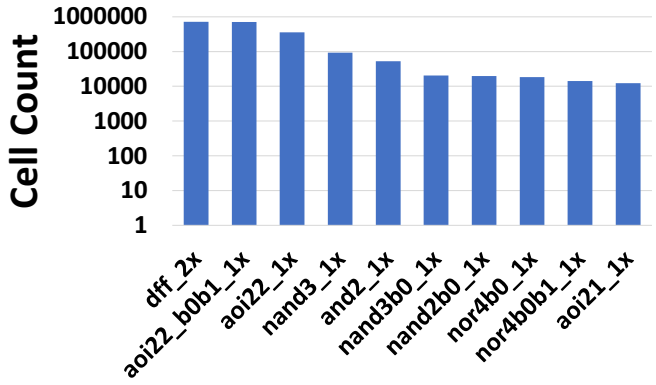
LIFETIME ASSESSMENT FLOW

In this chapter, circuit lifetime assessment flow is presented. Extraction of circuit operating conditions is discussed. The characterization of standard cell lifetime is presented in detail. Also, the full chip lifetime analysis incorporating with process, voltage and temperature variation is studied.

4.1 Extraction of Circuit Operating Conditions

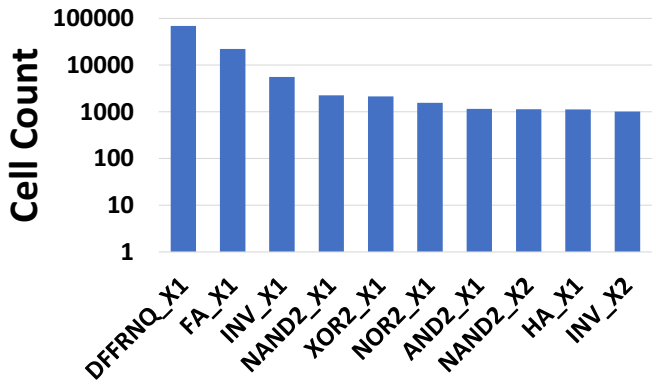


(a)

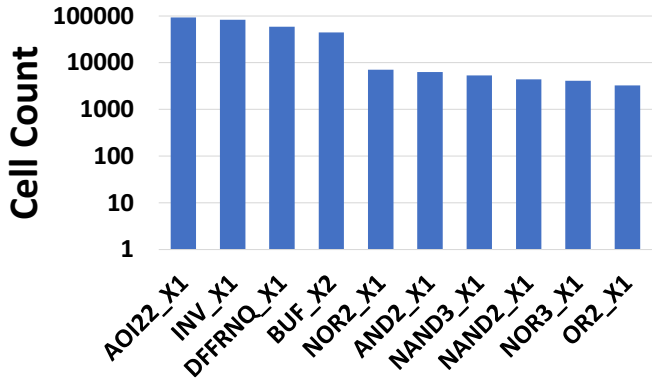


(b)

Figure 4.1: Counts of the top ten standard cells in traditional Bulk CMOS technology for the (a) FFT circuit and the (b) Leon3 microprocessor.



(a)



(b)

Figure 4.2: Counts of the top ten standard cells in FinFET CMOS technology for the (a) FFT circuit and the (b) Leon3 microprocessor.

In this section, we discuss the extraction of circuit operating conditions. As a vehicle for analysis, an 8-bit FFT circuit and a Leon3 microprocessor were implemented in the IBM 90nm process and the FreePDK15 [98] FinFET process in this study to demonstrate the functionality of our simulator. Synthesis was done with Synopsys Design Compiler [99]. For traditional bulk CMOS technology, the FFT circuit is composed of 22 types of standard cells and the Leon3 is composed of 54 types of standard cells. In the FinFET technology, the FFT circuit is composed of 38 types of standard cells and the Leon3 uses 18 types of standard cells. Counts of the top ten standard cells are shown in Figs. 4.1 and 4.2 for traditional bulk CMOS and FinFET CMOS, respectively.

For the target circuits, the method for standard cell characterization is presented, fol-

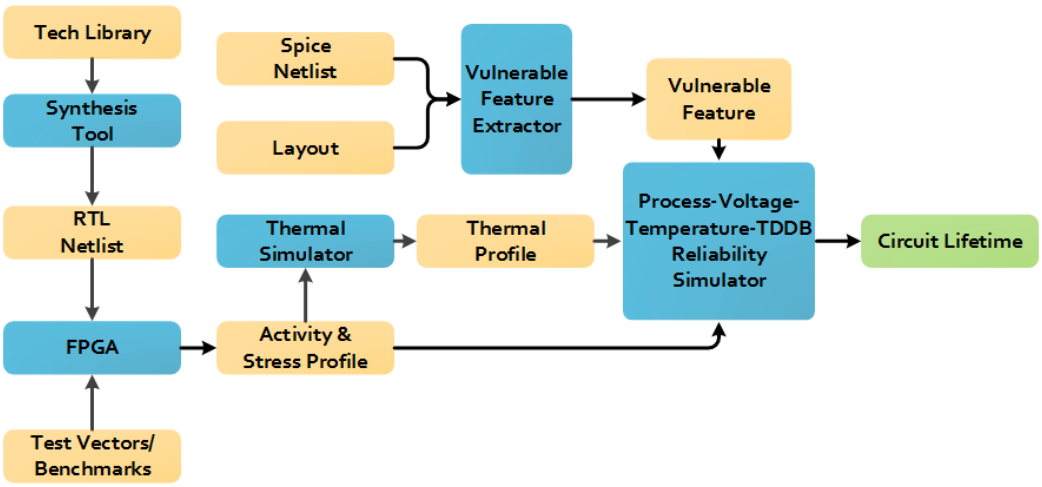


Figure 4.3: Framework for the reliability simulator. Yellow boxes are data and blue boxes are tools.

lowed by techniques to combine the lifetimes of the standard cells together to estimate the failure probability of the full circuit over time, while considering different operating conditions.

The framework of our reliability simulator is presented in Fig. 4.3. This figure describes the tool flow needed to compute lifetime. The left most part of the figure includes the tools needed to determine operating profiles, such as stress profile, duty cycle, and temperature for each cell in the circuit. The blocks in the middle combine operating profiles together to calculate lifetime. The lifetime is first computed for individual standard cells, and then these lifetimes are combined to find the total lifetime of the circuit.

For GOBD and MOL TDDB, the significant factors are the circuit stress profile, supply voltage (VDD), temperature, and the vulnerable features. For stress profile generation, the circuit netlist of the design was synthesized for an FPGA, and monitors were placed at the I/O ports, which can track both state probabilities and the toggle rate. Details for FPGA emulation can be found in [56]. We record the resulting state probabilities and toggle rates of the I/O ports and use PrimeTime [100] for activity propagation. After this step, we obtain the state probabilities and toggle rates for all the internal nets. The state probabilities are the key parameters to determine the lifetime of each vulnerable feature, since they determine

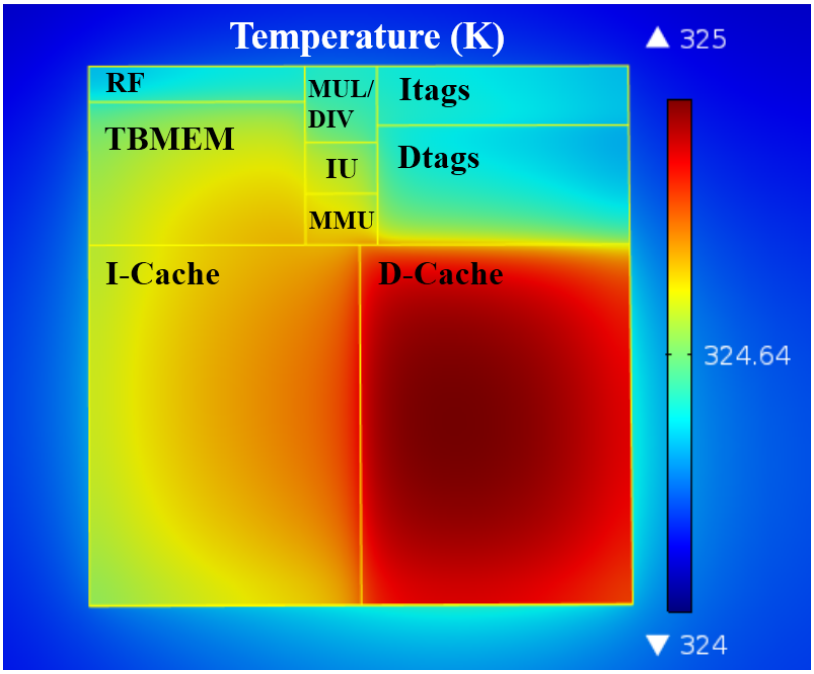


Figure 4.4: The average temperature distribution of Leon3 implemented in FinFET technology while running a standard benchmark.

the time that each feature is under stress.

Using the net activity and the RC information from the layout, we can find the power consumed by each component of the Leon3 microprocessor. To determine the thermal distribution, we consider the self-heating effects of the FinFETs and supply the power consumption data to COMSOL [101]. An example temperature distribution when the Leon3 is running a standard benchmark is shown in Fig. 4.4. The temperature profile is associated with every standard cell in the microprocessor. The variation in temperature is small because of the small size of the circuit.

The FFT circuit is supplied with randomly generated inputs and the circuit continuously performs the Fast Fourier Transformation (FFT) on the data. For the Leon3, we consider the degradation under different use scenarios, as shown in Fig. . Different use scenarios have their corresponding fractions of time when the system is in the three modes: operation, standby, and off. The stress profiles are determined by running standard benchmarks [103]. Our experimental results use a combination of standard benchmarks.

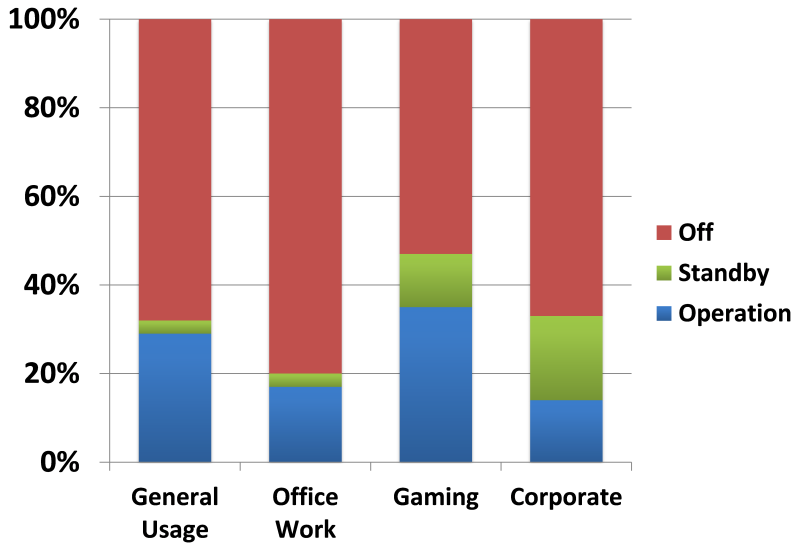


Figure 4.5: The use scenarios provided by Intel [102].

4.2 Standard Cell Lifetime Characterization

In this work, we consider variation in NMOS and PMOS channel length and variation in gate offset. Variation in channel length are mainly determined by accuracy in etch and photolithography. NMOS and PMOS devices are affected equally. Variation in gate offset is primarily determined by alignment between the gate and the contact masks. Both sources of variation are primarily die-to-die variations, rather than within-die variations. This means that all devices in a standard cell and all standard cells in a chip receive the same shift in parameters.

The channel length variation will cause the linespace to increase or decrease in the same direction, while the gate location offset will increase linespace on one side and decrease it on the other side, as shown in Fig. 3.3. Note that channel length variation only affects GOBD, while MOL TDDB is influenced by both sources of variation. In this work, we assume that variation is modelled with a normal distribution, with a standard deviation of 10% of nominal.

Pre-characterization of the standard cells requires that we consider all possible input probabilities and all possible die-to-die variations. Consider for example the add_1x1x cell

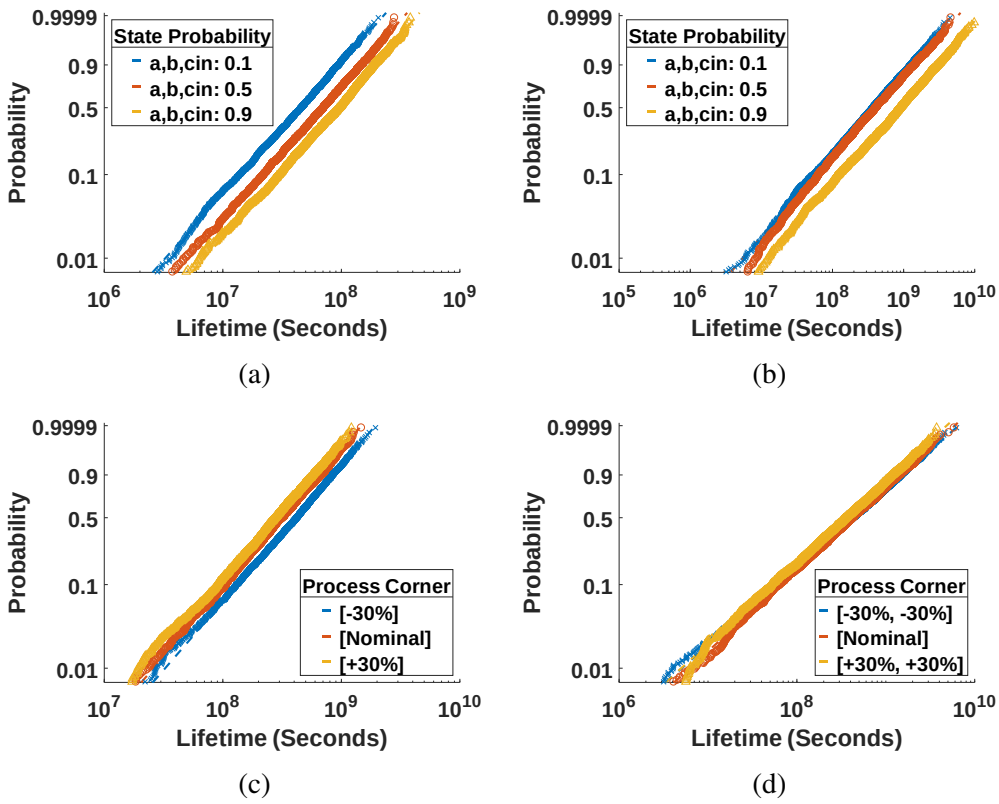


Figure 4.6: Traditional bulk CMOS standard cell (add_1x1x) lifetime distribution as a function of input state probability: (a) GOBD and (b) MOL TDDB; cell lifetime distribution as a function of process variations (inputs' state probability = 0.5): (c) GOBD with channel length variation and (d) MOL TDDB with channel length and gate offset variation. The vertical axis is the Weibull scale, i.e. ln(-ln(1-F)), where F is the cumulative probability of failure.

which has three inputs. Suppose that we partition the input state probabilities into five categories: 0-0.2, 0.2-0.4, 0.4-0.6, 0.6-0.8, and 0.8-1.0. Then for three inputs, we require that the cell is characterized for 5^3 possible input states. Die-to-die process parameter variation adds to the number of cases to be considered. Consider for example the channel length variation which is partitioned into seven states (-30%, -20%, -10%, 0%, 10%, 20%, 30%), then we need to characterize the add_1x1x cell for $7 \cdot 5^3$ cases for GOBD, and we need to characterize the add_1x1x cell for $7^2 \cdot 5^3$ cases. This characterization process is only done once for all possible die-to-die parameter shifts and for all possible input states. Example lifetime distributions for one of the cells in the traditional bulk CMOS technology

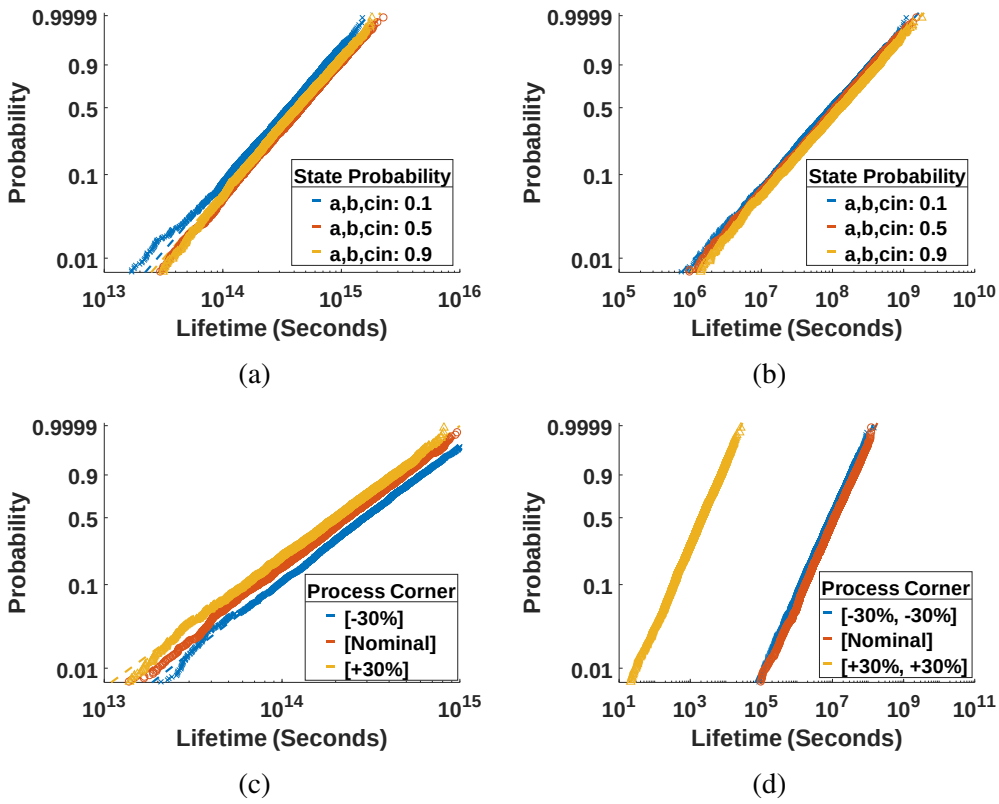


Figure 4.7: FinFET standard cell (FA: full adder) lifetime distribution as a function of input state probability: (a) GOBD and (b) MOL TDDB; cell lifetime distribution as a function of process variations (inputs' state probability = 0.5): (c) GOBD with channel length variation and (d) MOL TDDB with channel length and gate offset variation. The vertical axis is the Weibull scale, i.e. ln(-ln(1-F)), where F is the cumulative probability of failure.

(add_1x1x) and one of cells in FinFET technology (FA: full adder) are shown in Figs. 4.6 and 4.7.

We can see that the lifetime of each combination of input states does not cause a significant variation in the lifetime distribution. This can be explained by the complementary of the transistor. If an NMOS transistor is under stress, the PMOS is not under stress, and vice versa. Also, if one node is at logic "1", it stresses the dielectric between the node and ground, while if the node is at logic "0", it stresses the dielectric between the node and the supply voltage.

In Figs. 4.6(c), 4.6(d) and 4.7(c), we find that the process variation does not have a big impact on a cell's lifetime distribution. However, in Fig. 4.7(d), the MOL TDDB

Table 4.1: Computational Cost for Vulnerable Feature and State Probability Extraction

		CMOS	FinFET
FFT	GOBD Feature Extraction	0.78s	0.23s
	MOL TDDB Feature Extraction	12.63s	4.98s
	State Probability Extraction	13.41s	13.05s
	Total Number of Standard Cells	102k	112k
Leon3	GOBD Feature Extraction	1.94s	0.21s
	MOL TDDB Feature Extraction	31.01s	2.45s
	State Probability Extraction	55s	30.01s
	Total Number of Standard Cells	202k	312k

is extremely vulnerable to process variation. This can be explained by the small feature size in the FinFET layout. The minimum linespace in a FinFET standard cell is 8nm, and a 30% change in channel length will cause the linespace to reduce to 5nm; in addition, the gate location offset will make the linespace on one side to reduce more. Thus, the cell lifetime distribution under 30% length variation and 30% gate offset makes the cell extremely vulnerable to wearout.

The computational cost for vulnerable feature and state probability extraction for our simulator is shown in Table III. In our experiment, we use a PC with 3.4GHz Intel i7-6700 core CPU and 16GB memory. It can be seen in the Table III that MOL TDDB extraction and the total standard cell characterization takes more time for traditional bulk CMOS technology. This can be explained by the number of standard cells in our traditional bulk CMOS technology library, which is 628 and is larger than the 69 types of standard cells in our FinFET technology library. Also, we can find that when there are larger numbers of standard cells in the circuit, our simulator takes longer to extract the state probability. In Table IV, the computational cost for standard cell characterization is shown. The full adder takes more time to characterize than the inverter cell, since the full adder has three inputs and the inverter only has one. In addition, the characterization time increase if there are

Table 4.2: Computational Cost for Standard Cell Characterization

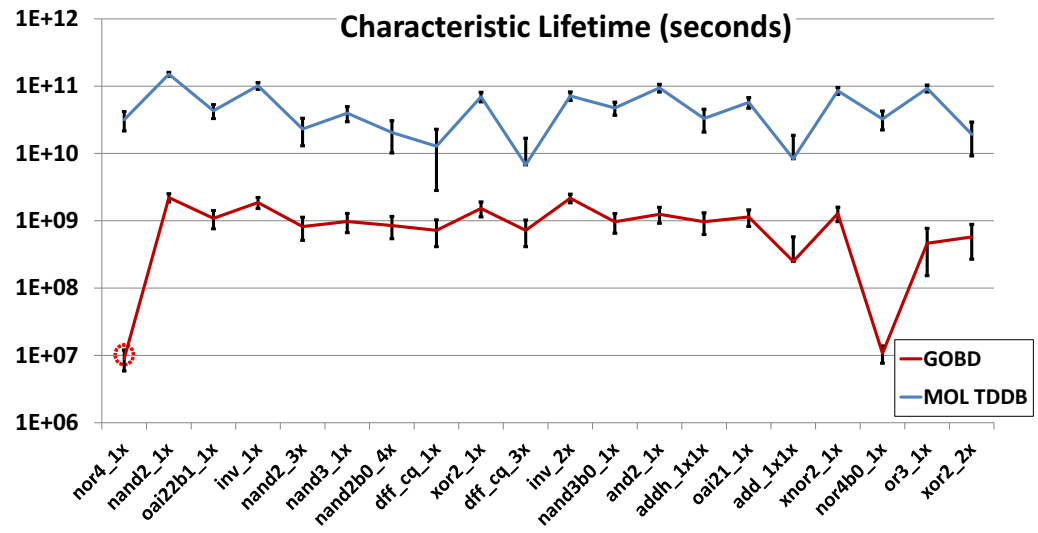
		Types of Standard Cell	GOBD	MOL TDDB	Total Time
CMOS	Full Adder	1	1.78s	3.63s	5.41s
	Inverter	1	1.07s	0.71s	1.78s
	FFT	22	31.35s	48.02s	79.37s
	Leon3	54	77.05s	118.23s	195.28s
FinFET	Full Adder	1	2.02s	1.38s	3.4s
	Inverter	1	1.06s	0.38s	1.44s
	FFT	38	58.12s	33.47s	140.79s
	Leon3	18	28.22s	16.21s	66.69s

more types of standard cells in the circuit.

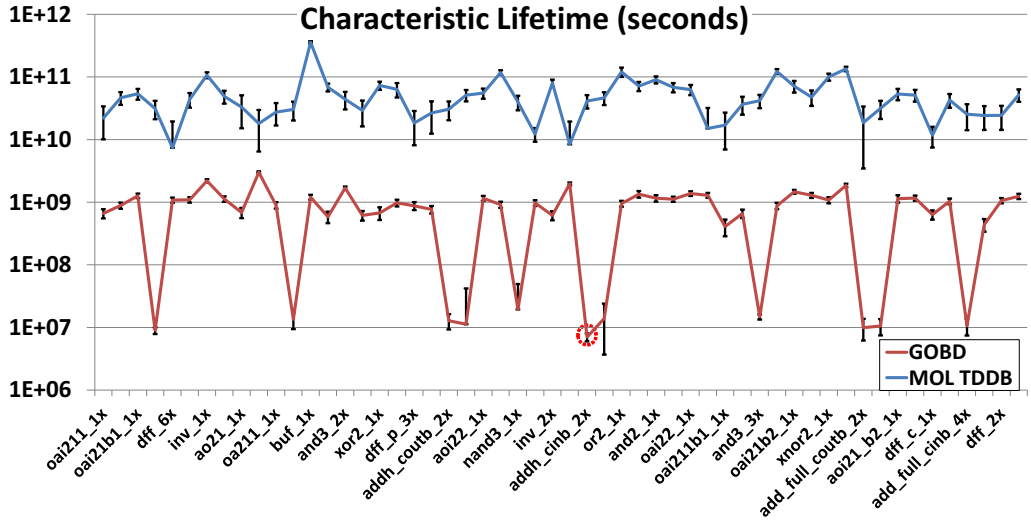
By using Eqs. (3.3) to (3.5), we can get the characteristic lifetime of GOBD and MOL TDDB for every standard cell in the FFT circuit and the Leon3 microprocessor, which are shown in Fig. 4.8 and Fig. 4.9 for traditional bulk CMOS and FinFET CMOS technology, respectively. The standard cell lifetime distributions are simply combinations of the transistor/vulnerable feature lifetimes of all the transistors and vulnerable features in the cell. The input probabilities for each logic state for the standard cell propagate to internal nodes within the cell and determine the stress probabilities of transistors and vulnerable features. The data in Fig. 4.8 and Fig. 4.9 are represented as a mean and standard deviation of each type of cell in the circuit. The variation is due to variation in use conditions.

Our simulator can locate the most vulnerable features in the lifetime limiting cells in FinFET technology. As shown in Fig. 4.10, we show half of the layout of the INV_X16 cell. We can find that the layout of INV_X16 is symmetrical and the reason it is the lifetime limiting cell is that there are more vulnerable features in this cell.

By inspecting the figures, we can find that GOBD dominates the lifetime for traditional bulk CMOS, while MOL TDDB plays an increasingly important role for FinFET technology. This is the expected result. Voltage scaling helps to alleviate the impact of GOBD for



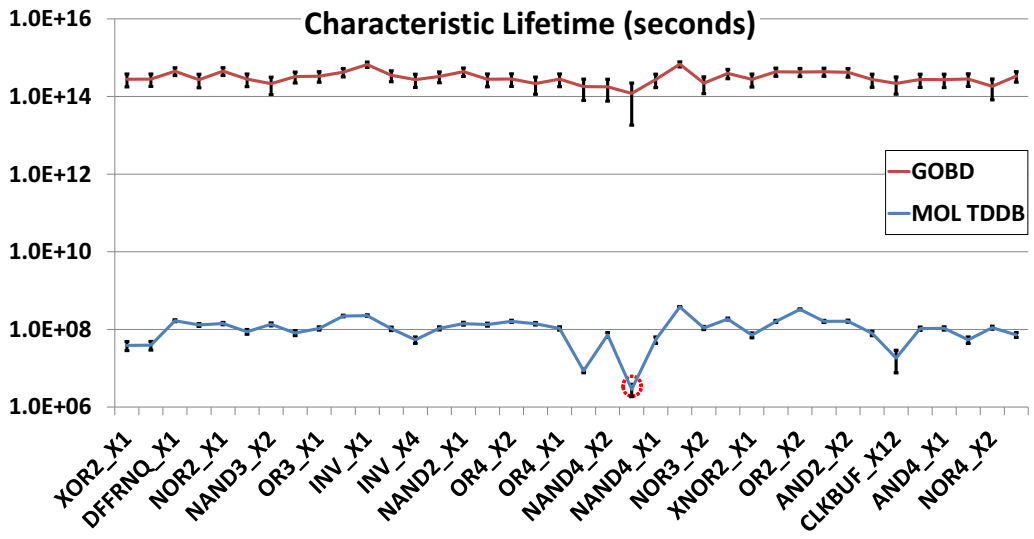
(a)



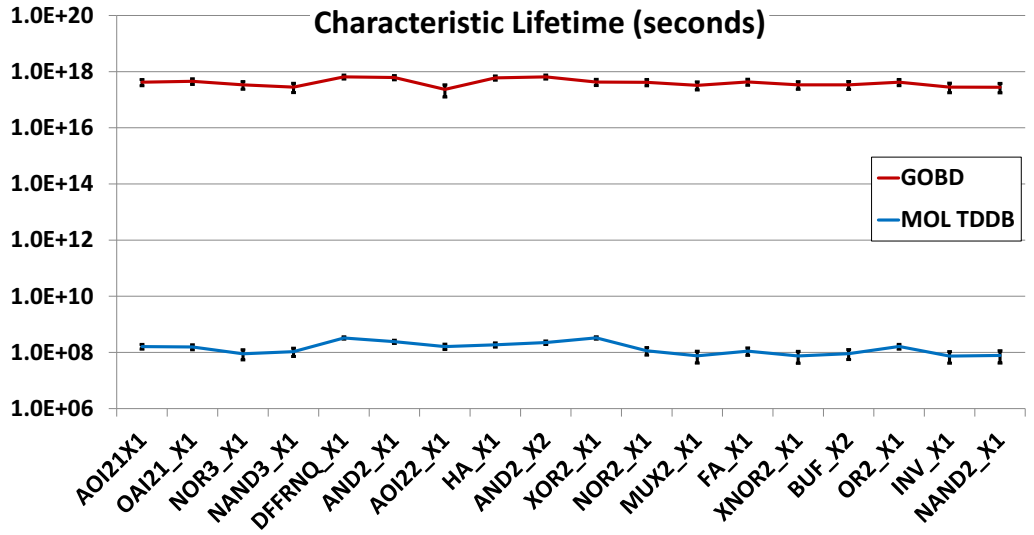
(b)

Figure 4.8: Traditional bulk CMOS standard cell characteristic lifetime under nominal process variation for GOBD and MOL TDDB for the (a) FFT circuit (nor4_1x is the lifetime limiting cell, shown in red dashed circle) and the (b) Leon3 microprocessor (comp_42_1x is the lifetime limiting cell, shown in red dashed circle). Variation is due to variation in operating conditions of the cells.

FinFET technology, while the more compact layout of FinFET technology leads to smaller distances between conductor which results in a worse lifetime. That is, the technology scaling has made the dielectric between gate and contact more vulnerable than ever.



(a)



(b)

Figure 4.9: FinFET CMOS standard cell characteristic lifetime under nominal process variation for GOBD and MOL TDDB for the (a) FFT circuit (INV_X16 is the lifetime limiting cell, shown in red dashed circle) and the (b) Leon3 microprocessor.

4.3 Full Chip Lifetime Analysis

To find the full chip lifetime, we first combine different standard cell lifetime distributions together using Eqs. (3.3) to (3.5). The lifetime distributions are combined together for each shift in process parameters. Hence, if there are seven categories for channel length

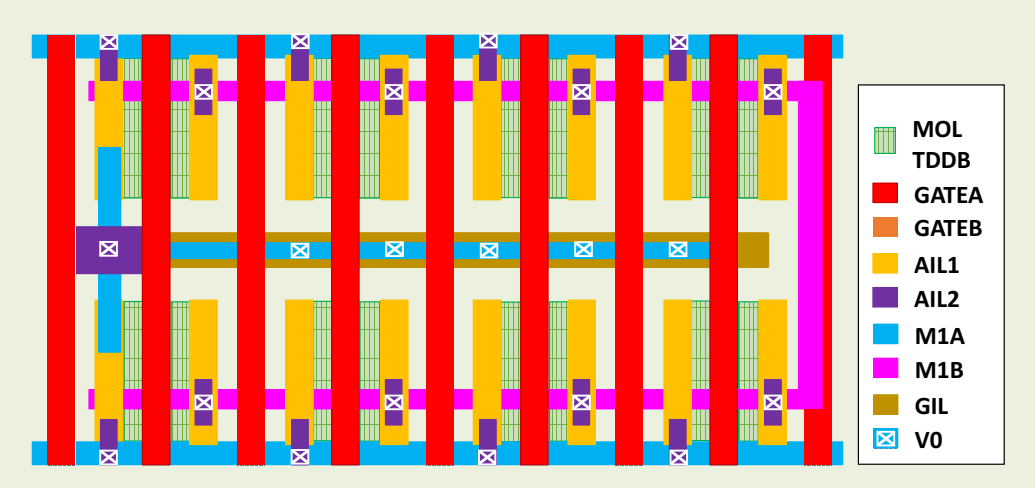


Figure 4.10: Vulnerable features of the lifetime limiting INV_X16 cell in FinFET techonology (only half of the layout is shown).

variation, then for GOBD there are seven lifetime distribution, one for each of the categories. For MOL TDDB, since there are two parameters, channel length and offset, with seven categories each, then the lifetime distribution for the full chip is computed for all 49 categories. The combination of the lifetime distribution takes into account the input state probabilities associated with the benchmark running on the circuit.

The next step is to combine the lifetime distributions according to the distribution of the process parameters. For example, if the die-to-die channel length variation is normal with a standard deviation of 10%, then when combining the lifetime distributions for GOBD, 0.62% of the points will come from the each of the -30% and +30% shift distributions, 6.06% of the points will come from the -20% and +20% shift distributions, 24.17% of the points from the -10% and +10% shift distributions, and 38.3% of the points from the nominal distribution. The distributions are similarly combined for MOL TDDB. The results are shown in Fig. 4.11 and Fig. 4.12. It can be seen that when combining normally distributed process variations with a Weibull distribution for the wearout mechanism, the result is not quite a Weibull distribution. Data from extreme points on the Normal distribution, produce the points in the tails of the distribution, where the lifetime is less than would be expected with a Weibull distribution.

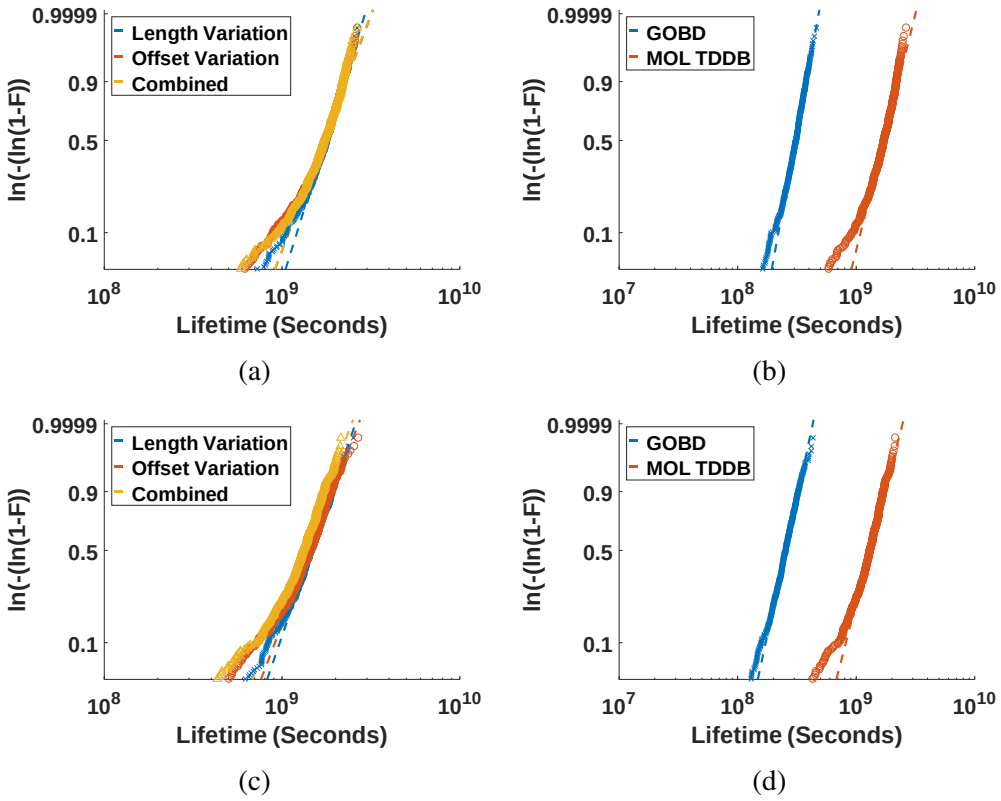


Figure 4.11: Lifetime distributions for the full FFT chip for traditional bulk CMOS incorporating process variations, (a) for MOL TDDB, comparing the impact of different components of process variation, and (b) comparing GOBD and MOL TDDB. Lifetime distributions for the Leon3 microprocessor incorporating process variations (c) for MOL TDDB, comparing the impact of different components of process variation, and (d) GOBD and MOL TDDB. The vertical axis is the Weibull scale, i.e. ln(-ln(1-F)), where F is the cumulative probability of failure.

Figs. 4.11 and 4.12 can be compared to see the impact of technology scaling. The trend indicates the increasing importance of MOL TDDB. However, because this study is based on limited experimental data, one cannot conclude that MOL TDDB is more important than GOBD. It can only be claimed that it is becoming a greater concern for advanced technology nodes implemented with FinFETs. Notice also that process variations have a greater impact on circuit lifetime for FinFET technology, which is aligned with the previous analysis for Fig. 4.7(d).

To calculate the probability of failure at time t for each circuit, we use the Weibull distribution, with characteristic lifetime, η, and shape parameter, β. The probability of

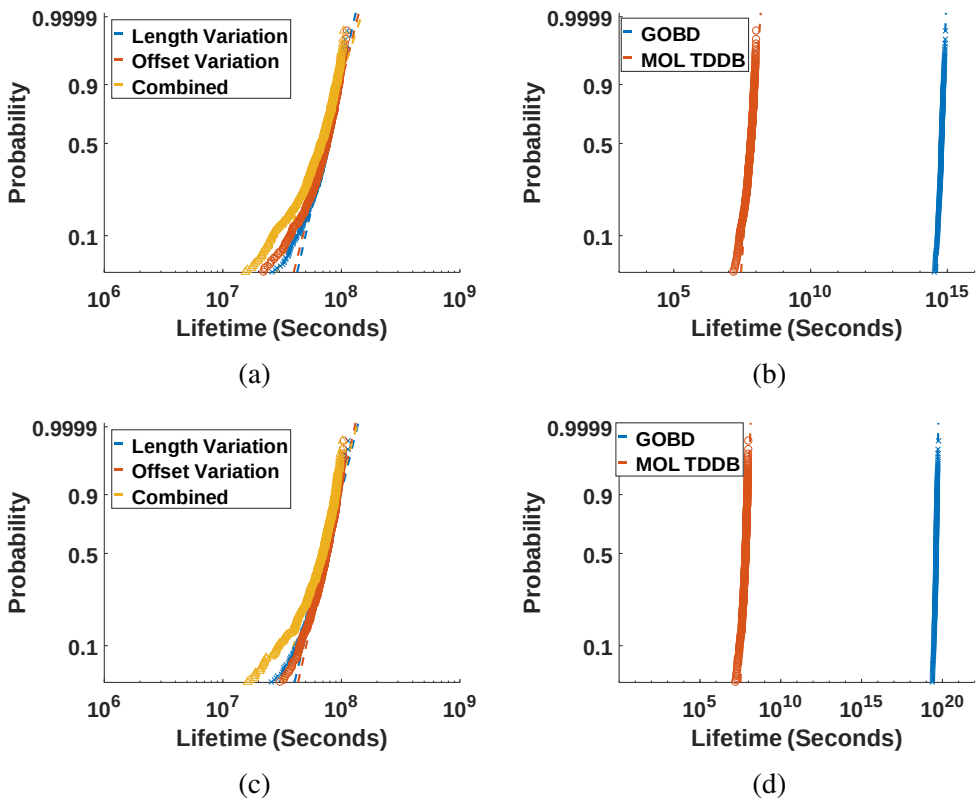


Figure 4.12: Lifetime distributions for the full FFT chip for FinFET CMOS incorporating process variations, (a) for MOL TDDB, comparing the impact of different components of process variation, and (b) comparing GOBD and MOL TDDB. Lifetime distributions for the Leon3 microprocessor incorporating process variations (c) for MOL TDDB, comparing the impact of different components of process variation, and (d) GOBD and MOL TDDB. The vertical axis is the Weibull scale, i.e. ln(-ln(1-F)), where F is the cumulative probability of failure.

failure at time t is calculated by Eq. (3.7).

The resulting failure probability vs. time is shown in Fig. 4.12. Notice that, in bulk CMOS technology, the FFT circuit in Fig. 4.12(a) fails more slowly than the Leon3 microprocessor in Fig. 4.12(b) (has a lower failure probability at each time point), while in FinFET technology, the FFT circuit in Fig. 4.12(c) has a shorter lifetime in comparison with the Leon3 microprocessor in Fig. 4.12(d) (fails faster than the Leon3 microprocessor). Although the FFT circuit uses fewer standard cells, we find in Fig. 4.9(a), that there is lifetime limiting cell shown with dashed red circle. This type of cell (INV_X16) causes the FinFET FFT circuit to have a shorter lifetime than the Leon3, despite the fact that it is

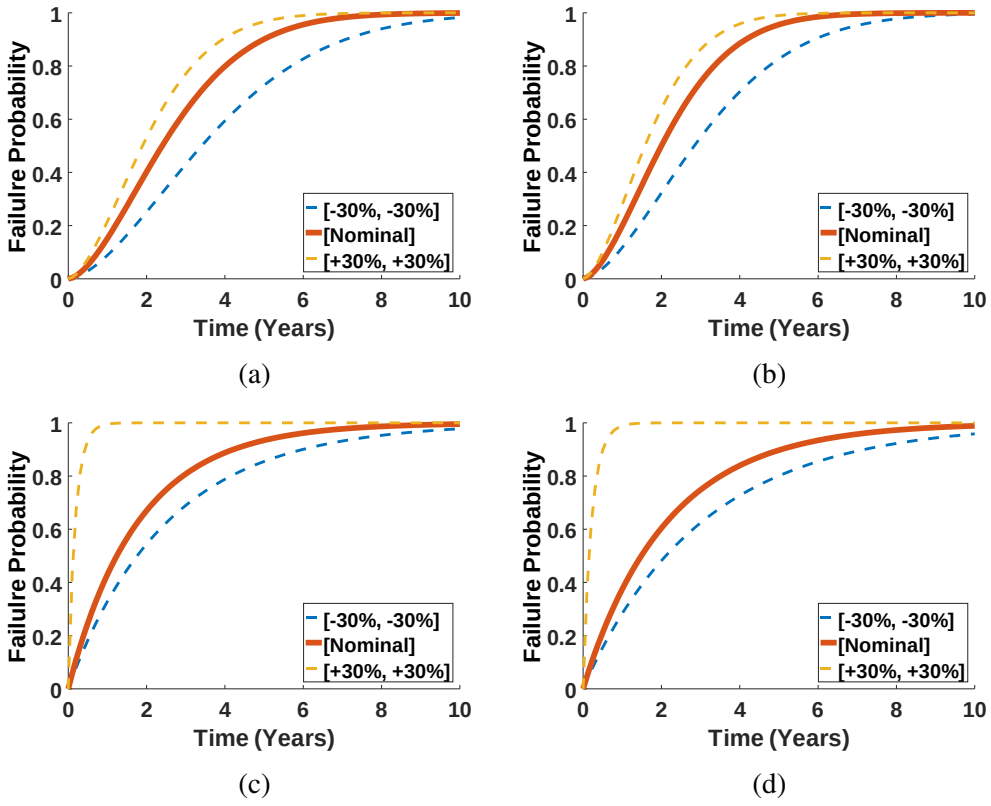
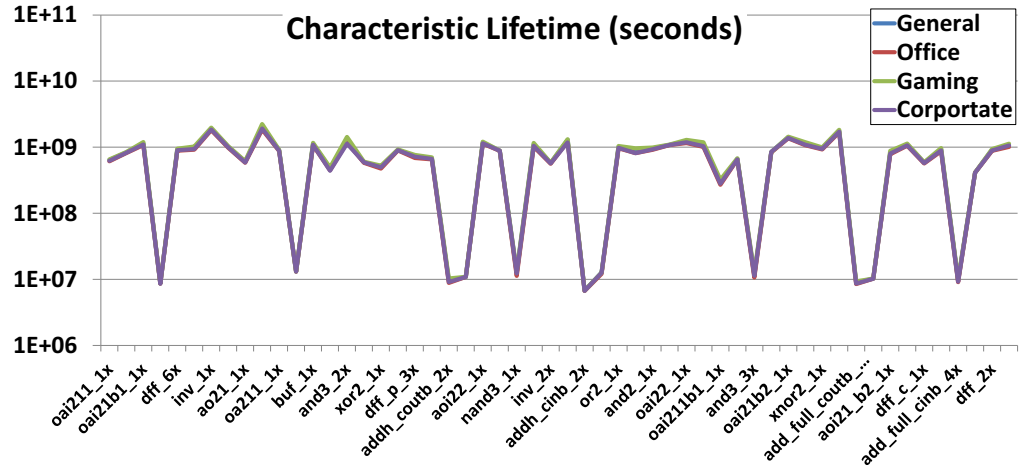


Figure 4.13: Failure probability for different circuits and technologies: (a) Traditional bulk CMOS FFT (b) bulk CMOS Leon3 (c) FinFET FFT and (d) FinFET Leon3. The dashed lines are for process corners.

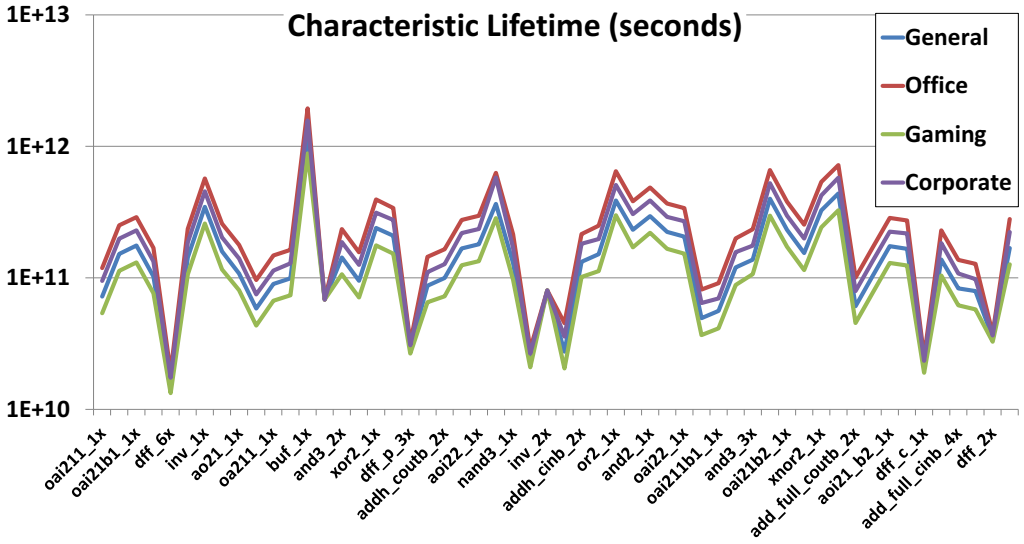
a much smaller circuit.

To analyze the impact of the use scenario on the Leon3, the stress during operation is computed based on activities when the Leon3 runs a standard benchmark. It idles with a random state in standby mode and powers down for the off mode. Substituting the stress profile into our simulator, we can compute the characteristic lifetime for different use scenarios, shown in Figs. 4.14 and 4.15. We can conclude that MOL TDDB is more sensitive to use scenarios while, as observed in Fig. 4.14(a) and Fig. 4.15(a), GOBD is not sensitive. The vulnerable features in MOL TDDB are associated with two nets in a standard cell, while for GOBD, each device is only associated with its gate voltage; and thus, the disturbance of two nets for MOL TDDB will have a larger impact than just one for GOBD.

In addition, one can find from Figs. 4.14 and 4.15 that not all standard cells have



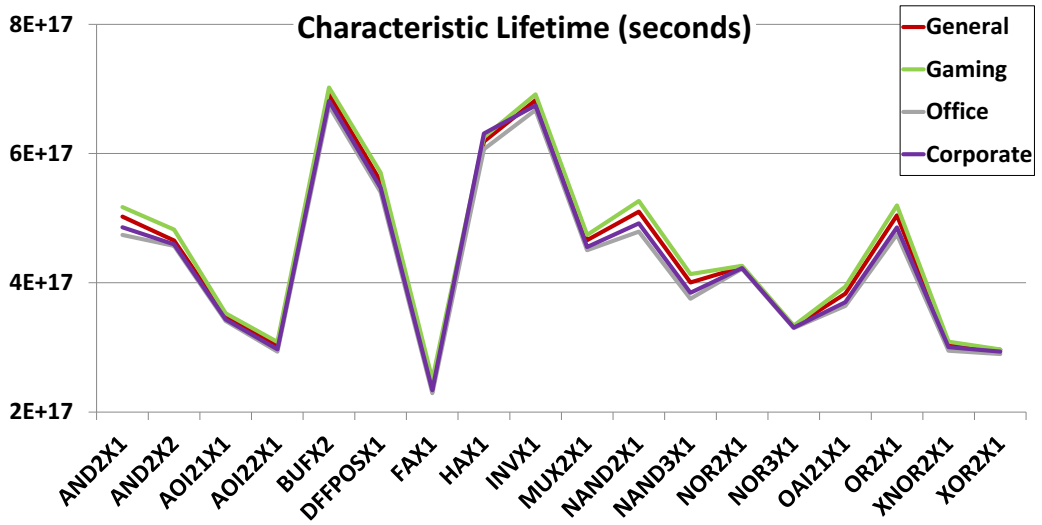
(a)



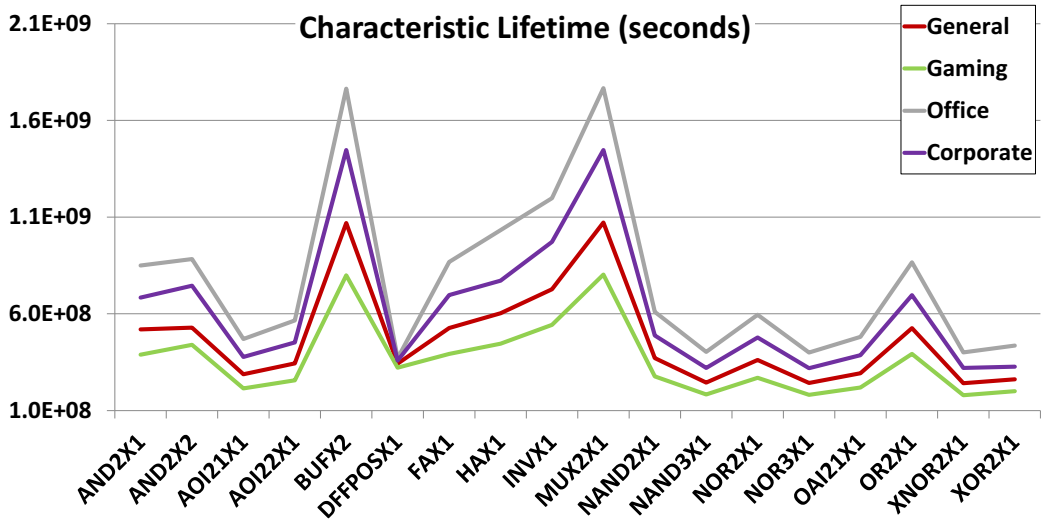
(b)

Figure 4.14: Variation in characteristic lifetime for nominal process parameters for the standard cells of the Leon3 microprocessor implemented in traditional bulk CMOS considering (a) GOBD and (b) MOL TDDB.

the same lifetime degradation under different use scenarios. With this information, it is possible for a circuit designer to choose specific types of cell over others to ensure a longer lifetime for specific applications.



(a)



(b)

Figure 4.15: Variation in characteristic lifetime for standard process parameters for standard cells of the Leon3 microprocessor implemented in FinFET CMOS, considering (a) GOBD and (b) MOL TDDB.

4.4 Conclusion

The simulator convers not only the traditional reliability concern, GOBD, but also the newly emerging wearout mechanism, MOL TDDB. A TDDB lifetime simulator for both traditional bulk CMOS and FinFET technology is proposed for the target wearout mecha-

nisms. The shrinking feature size in FinFET technology leads to severe degradation caused by MOL TDDB because of its sensitivity to alignment errors. On the other hand, voltage scaling alleviates the impact of GOBD and MOL TDDB. Process variation is taken into consideration and becomes a significant factor affecting a circuits' lifetime distribution.

With reliability simulation, a circuit designer can use the information to redesign a circuit or to redraw the layout in a more robust and reliable way; also, a circuit designer can use application specific information to choose certain cells that have longer lifetimes than others. It is also possible to use the lifetime information to add some constraints on circuit design to ensure the circuit's performance over the product lifetime.

The simulator introduces a methodology to identify the lifetime limiting cells in a circuit; optimization on the trade-off between power, area and lifetime of a circuit needs further investigation.

CHAPTER 5

PARAMETER ESTIMATION FOR WEAROUT MODELS

Accelerated life tests (tests at high voltages and temperatures) are often applied to stress CMOS circuits to assess their lifetimes. Device level degradation models enable the possibility to test at accelerated conditions and to predict the circuit's lifetime at normal operating conditions. More importantly, accelerated tests can be used to tell which wearout mechanism is dominant in a target circuit; and circuit designers can use such information to improve and redesign their circuits for robust operations and a longer lifetime.

Device-level degradation models act as a link from transistor to circuit-level lifetime results; and thus, the more accurate the parameters of device-level models are, the more accurate the final lifetime prediction result will be. To obtain accurate model parameters, we need to decouple different wearout mechanisms while testing, i.e., to test at certain conditions where only one wearout mechanism is dominant.

This leaves us with the task to find the optimal test conditions for each of these wearout mechanisms. We would like to test the circuit with the corresponding test conditions where only one wearout mechanism is likely to happen and we can then use these data to obtain the parameters of the wearout model via measurements on circuits.

5.1 Errors in Estimating Wearout Parameters at System-Level Accelerated Life Test Conditions

Fig. 5.1 shows wearout distributions obtained from system-level accelerated life test. There are two sources of errors. First, there are errors in estimating the Weibull distribution at accelerated conditions. Second, there are errors in estimating Weibull distribution at the use conditions. The first type of error relates to the parameters of the thin solid curves at accelerated test conditions, reflected in estimating β,η_1,η_2....The second type of error

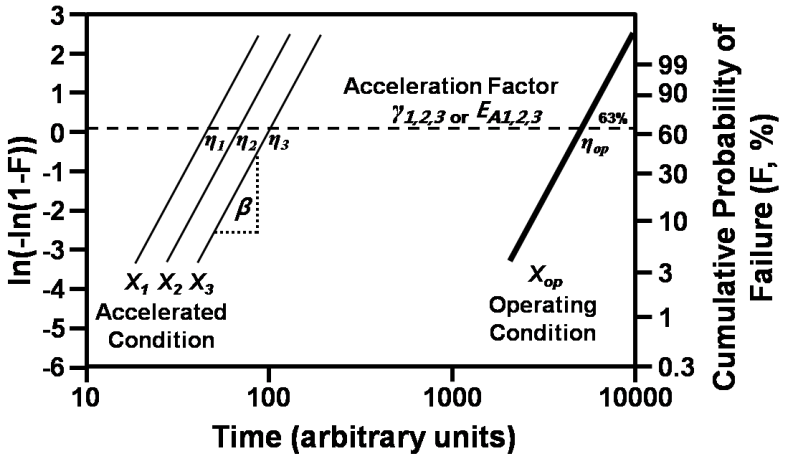


Figure 5.1: Errors in estimating a Weibull distribution at the operating condition using system-level accelerated life test: errors in the estimation of Weibull parameters at (1) accelerated conditions and (2) the operation condition. The thin solid lines reflect the collected data at the accelerated test conditions and the thick solid line reflects the predicted wearout distribution at use conditions.

relates to errors in estimating errors at use conditions which is depicted by the thick solid line.

During testing, we monitor the time-to-failure at high stress test conditions for accelerating breakdown in dielectrics. At each test point, we fit measured data to a Weibull distribution by employing an estimator, such as least squares or maximum likelihood regression.

Figs. 5.2 and 5.3 give the errors in estimating $log(\eta)$ and β respectively, with a one-sided 95% confidence interval, calculated using Monte Carlo simulation with the generalized maximum likelihood method for estimation [104]. The terms $\epsilon_{log(\eta)}$ and ϵ_β are relative errors, so that the results are independent of units. If we increase the number of samples, the accuracy in estimation $log(\eta)$ and β will also increase.

We define the probability that a mechanism will fail first within a certain test time limit as the selectivity of that specific wearout mechanism at the corresponding voltage and

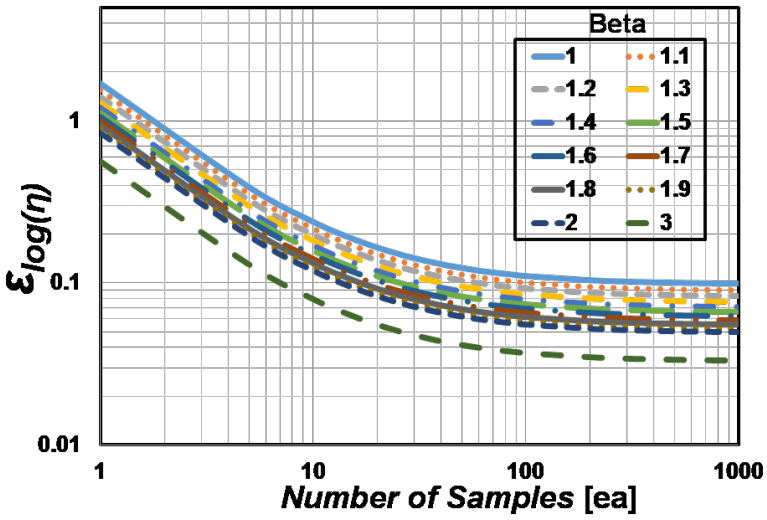


Figure 5.2: Relative errors in estimating $log(\eta)$.

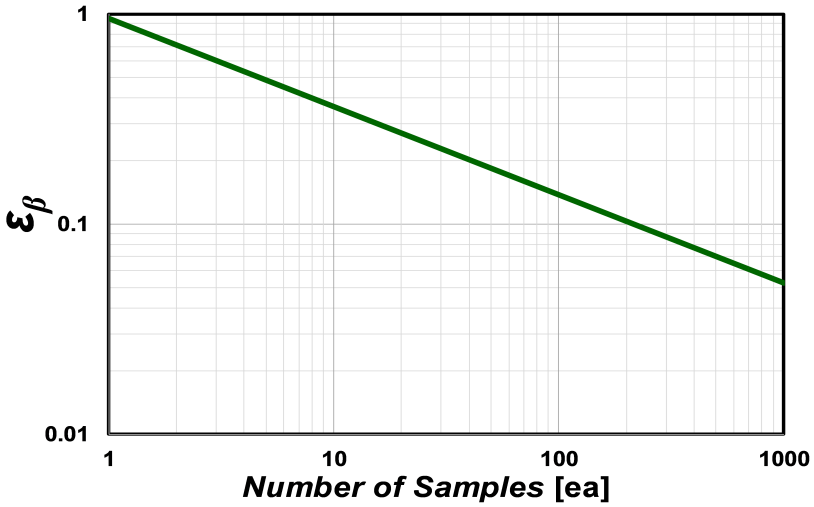


Figure 5.3: Relative errors in estimating β.

temperature,

$$Prob_{x\_fail\_first} = \int_0^{t_{stop}} Prob(x < Y | Y = y) f_y dy \tag{5.1}$$

To calculate the errors in estimating Weibull parameters, we employ a binomial distribution to model errors caused by selectivity. To estimate such errors in estimating $log(\eta)$

caused by selectivity, $\epsilon_{log(\eta)-selectivity}$, we employ the Wilson interval as follows [104]

$$\Delta\hat{p} = \frac{2z}{1+\frac{1}{n}z^2}\sqrt{\frac{1}{n}\hat{p}(1-\hat{p}) + \frac{1}{4n^2}z^2} \tag{5.2}$$

where $\hat{p}$ is selectivity of a target wearout mechanism at a test condtion, n is the total number of TDDB failures detected at a test condition, and z is the standard normal random variable ($z = 1.96$ at a 95% confidence interval). The Wilson interval is a more accurate confidence interval for binominal variable, $\hat{p}$.

From Eq. (5.1), the estimated selectivity $\hat{p}$ resulting from a target wearout mechanism ranges from $[\hat{p_l}, \hat{p_u}]$, yielding variation in the cumulative probability of failure due to the target wearout mechanism, F, at a test condition,

$$F = \frac{n}{N}\hat{p} \tag{5.3}$$

where N is the total number of circuits under test. Because of variation in $\hat{p}$, the cumulative probability of failure, F, is also a random variable, and $F_l = n\hat{p_l}/N$ and $F_u = n\hat{p_u}/N$ are the lower and upper confidence bounds respectively.

Variation in $\hat{p}$ causes variation in the cumulative probability of failure, F. This variation causes variation in characteristic lifetime η,

$$\Delta ln(\eta) = ln(\eta_l) - ln(\eta_u) = \frac{1}{\beta}ln(\frac{ln(1-\frac{1}{\hat{p_l}}+\frac{1}{e\hat{p_l}})}{ln(1-\frac{1}{\hat{p_u}}+\frac{1}{e\hat{p_u}})}) \tag{5.4}$$

If we set $z = 1$ in Eq. (5.1), then $\epsilon_{log(\eta)-selectivity} = \Delta log(\eta)/2$.

We can obtain $\epsilon_{ln(\eta)-sample}$ from Fig. 5.2, and thus, the total errors in estimating η can be expressed as,

$$\epsilon_{ln(\eta)} = \sqrt{{\epsilon_{ln(\eta)-sample}}^2 + {\epsilon_{log(\eta)-selectivity}}^2} \tag{5.5}$$

5.2 Optimal Accelerated Test Region

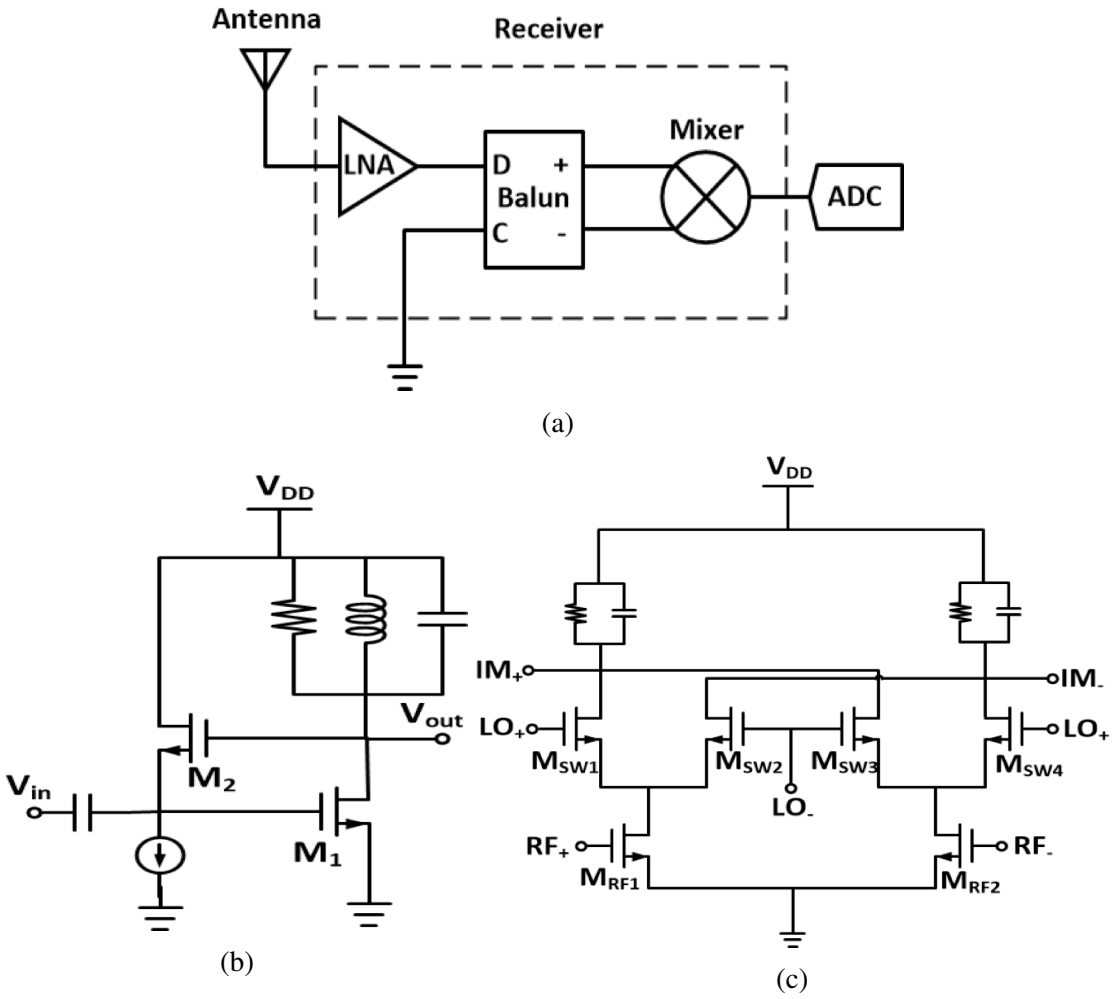


Figure 5.4: Radio frequency system (a) Receiver system diagram (b) low noise amplifier (c) Gilbert-Cell mixer.

To find the optimal accelerated test region, we simulate errors in estimating characteristic lifetime, η, for FEOL and MOL TDDB at accelerated conditions respectively and select the test area with the minimum estimation error for corresponding wearout mechanism.

In this study, we explore the optimal test region for three digital circuits. A 101-stage ring oscillator, an 8-bit FFT circuit and a Leon3 microprocessor were implemented in NCSU FreePDK15 FinFET technology [98]. Also, for analog circuit, we find the optimal test region for a receiver system, shown in 5.4. The FFT circuit consists of 112k cells and

the Leon3 microporcessor has 312k cells. The layout of Leon3 microprocessor is shown in Fig. 5.5.

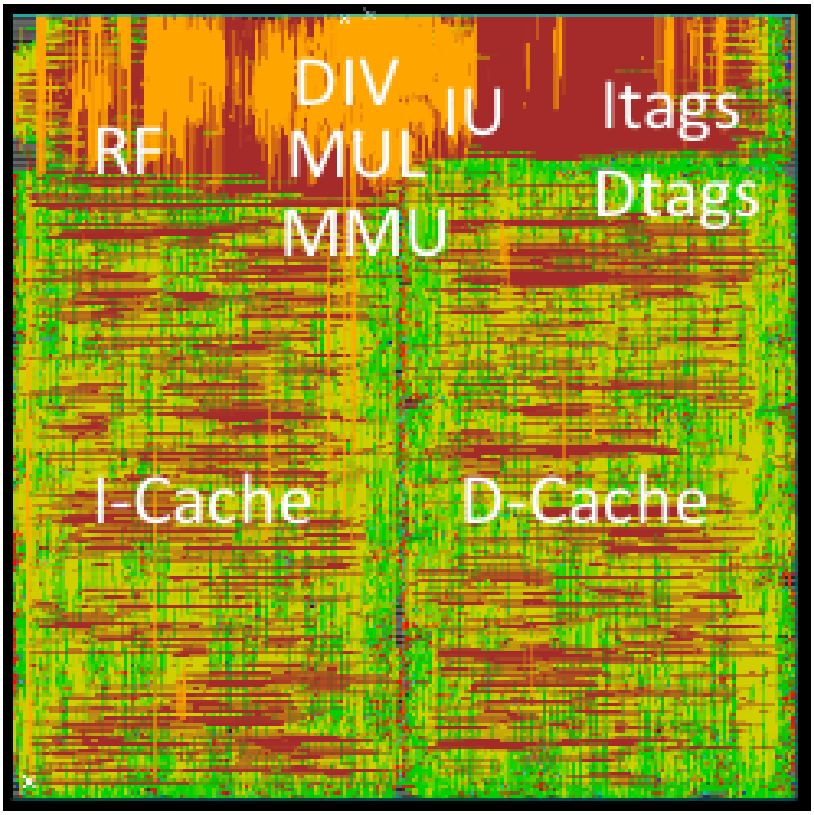
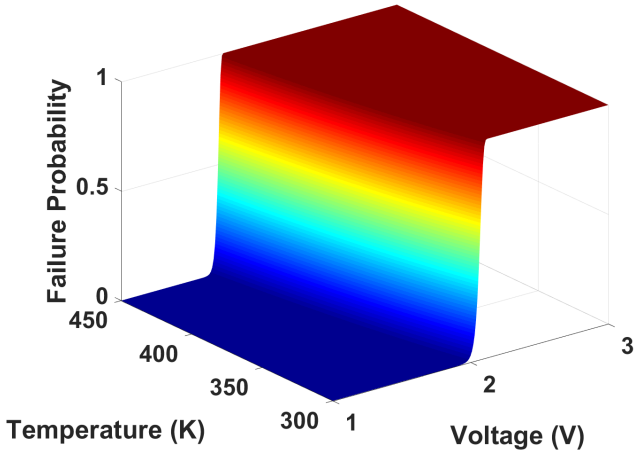


Figure 5.5: Leon3 microprocessor.

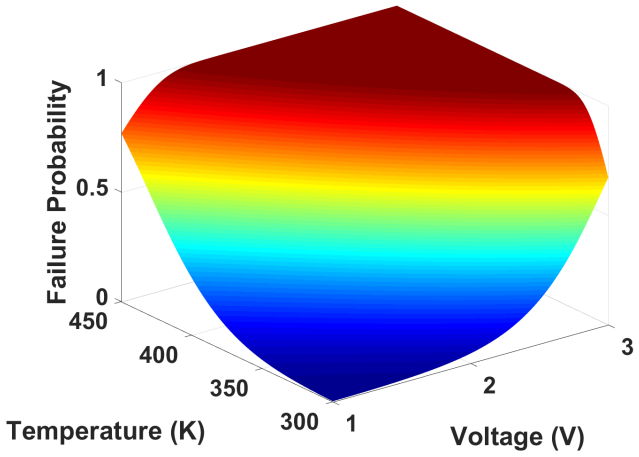
5.2.1 Probability to Fail First in the Whole Test Domain

We use Eq. (3.1) and Eq. (3.2) to calculate the characteristic lifetime of each vulnerable feature in the circuit and use Eqs. (3.3) to (3.5) to combine the individual characteristic lifetimes to get the whole circuit characteristic lifetime under FEOL and MOL TDDB. By applying Eq. (3.7), we can find the failure probability of the target wearout mechanism. And we perform the integration in 5.1 to get the probability of FEOL and MOL TDDB to fail first under every test condition with a 2-week test time. Results for bulk CMOS circuits can be found in Figs. 5.6, 5.7, 5.18 and 5.24 for the ring oscillator and Figs. 5.8, 5.9, 5.19 and 5.25 for the FFT circuit, and Figs. 5.10, 5.11, 5.20 and 5.26 for the receiver system; also, for FinFET technology, results can be found in Figs. 5.12, 5.13, 5.21 and 5.27 for

the ring oscillator Figs. 5.14, 5.15, 5.22 and 5.28 for the FFT circuit Figs. 5.16, 5.17, 5.23 and 5.29 for the Leon3 microprocessor.



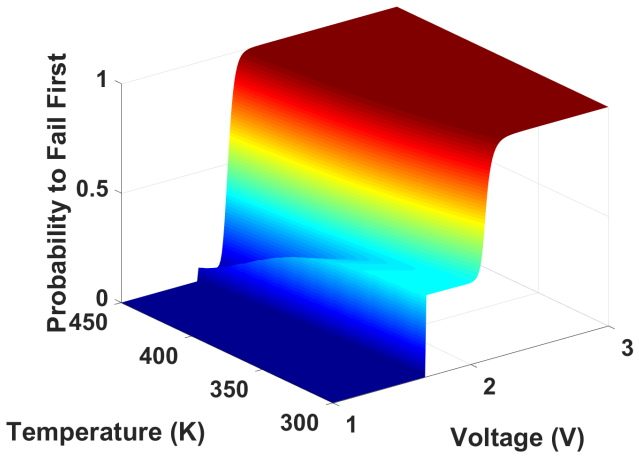
(a)



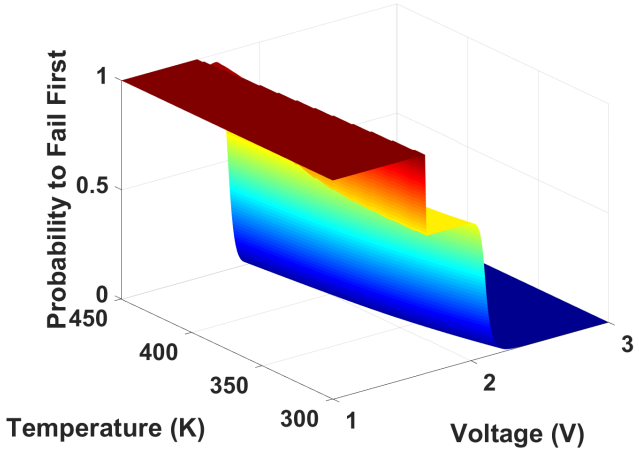
(b)

Figure 5.6: Failure probability of the ring oscillator in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

For the ring oscillator built in bulk CMOS technology, the failure of GOBD begins to happen at around 2V for low temperature and 1.5V for high temperature. For MOL TDDB, increasing the temperature has a larger effect on accelerating the failure, as we can find the slope is steeper along the temperature axis. The result is depicted in Fig. 5.6. For the selectivity (probability to fail first) of GOBD, we can find the probability begins to increase at around 2V shown in 5.7.



(a)

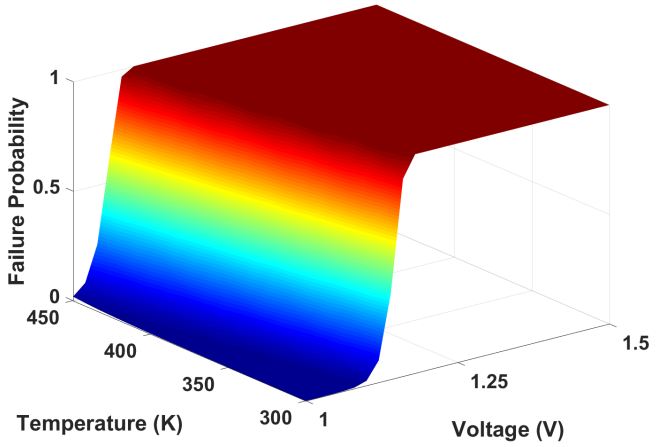


(b)

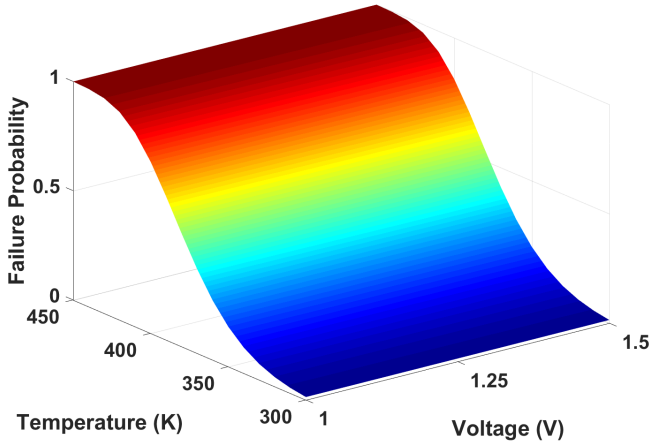
Figure 5.7: Selectivity of the ring oscillator in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

For the 8-bit FFT circuit implemented in bulk CMOS technology, since there are more standard cells in the circuit, it shows a lower voltage to begin to fail for GOBD, shown in Fig. 5.8(a). Also, in Fig. 5.8(b), we can find that MOL TDDB is not sensitive to low voltage, and thus, it is better to increase the temperature to accelerate the failure. In addition, the corresponding selectivity of GOBD and MOL TDDB for the FFT circuit can be found in Fig. 5.9. From the figure, we can conclude that it is better to test GOBD at higher voltage while to test MOL TDDB at a higher temperature.

As for the analog circuit in bulk CMOS technology, the failure probability of GOBD



(a)

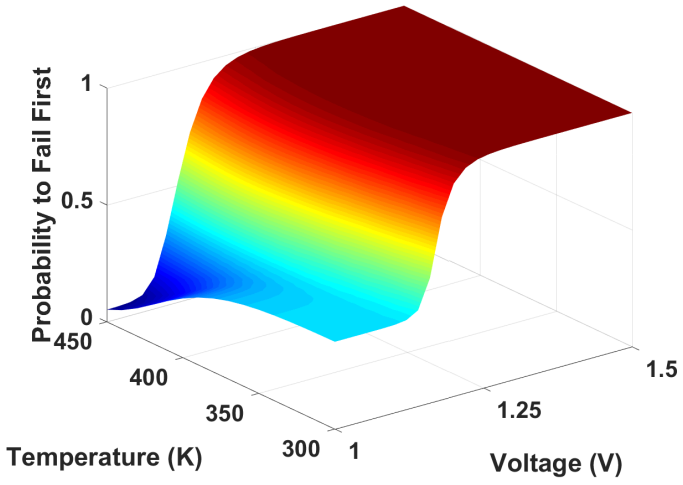


(b)

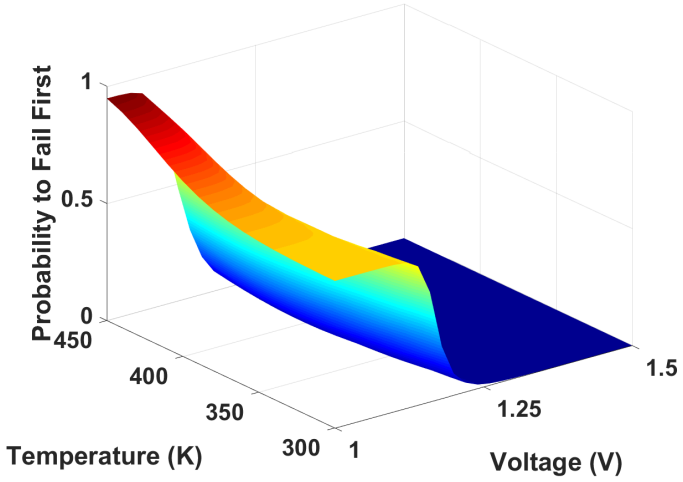
Figure 5.8: Failure probability of the FFT circuit in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

and MOL TDDB for the receiver system are shown in Fig. 5.10. In Fig. 5.10(a), we can find that the analog circuit is less sensitive to voltage (fails at higher voltage). This can be explained by most of the transistors in the receiver do not sustain the rail-to-rail voltage stress. As we expect, MOL TDDB is more sensitive to temperature as depicted in Fig. 5.10(b). By doing the integration in Eq. (5.1), we obtain the selectivity in Fig. 5.11.

In FinFET technology, the failure probability of ring oscillator is depicted in c5.12. As we can see, since the transistor size is smaller, GOBD failure is move to higher voltage while MOL TDDB is more severe in FinFET technology. Thus, to test GOBD in FinFET



(a)

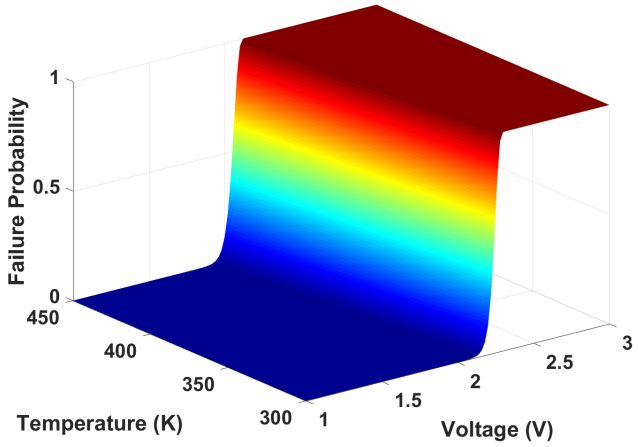


(b)

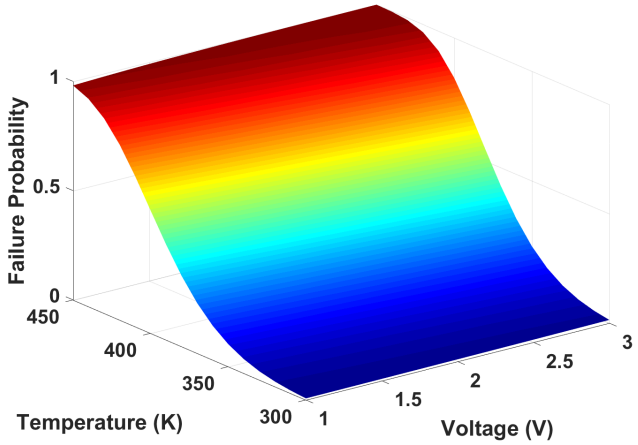
Figure 5.9: Selectivity of the FFT circuit in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

technology for ring oscillator, we need to move our test region into the higher voltage domain and it would be easier to test MOL TDDB in FinFET technology. The selectivity is shown in Fig. 5.15.

For the 8-bit FFT circuit in FinFET technology, since there are around 112k cells in the circuit, the circuit failure due to GOBD still happens at relative low voltage domain. As for MOL TDDB, compare to Fig. 5.8(b), we can find in Fig. 5.14(b) that MOL TDDB is more sensitive for temperature. Also, the corresponding selectivity for GOBD and MOL TDDB



(a)

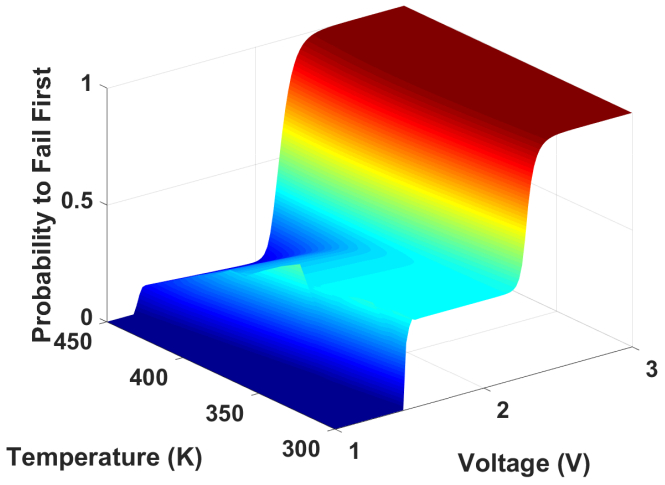


(b)

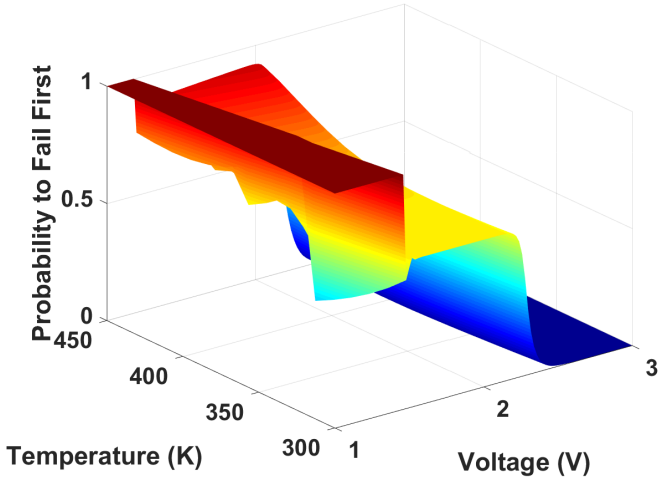
Figure 5.10: Failure probability of the receiver system in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

are shown in 5.15.

To demonstrate our simulator can determine the optimal test region for more complex systems, we also obtain the optimal test region for the state-of-art Leon3 microprocessor. Since the Leon3 microprocessor uses different standard cell types from the FFT circuit, the failure for GOBD happens at higher voltage, shown in Fig. 5.16(a). For MOL TDDB, we can observe similar trend, that temperature will be the main factor to accelerate the failure in Fig. 5.16(b). Also, we do the integration in Eq. (5.1) to get the selectivity in 5.17.



(a)

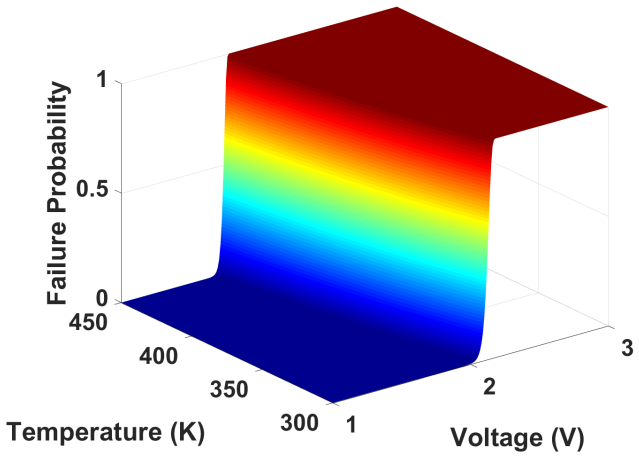


(b)

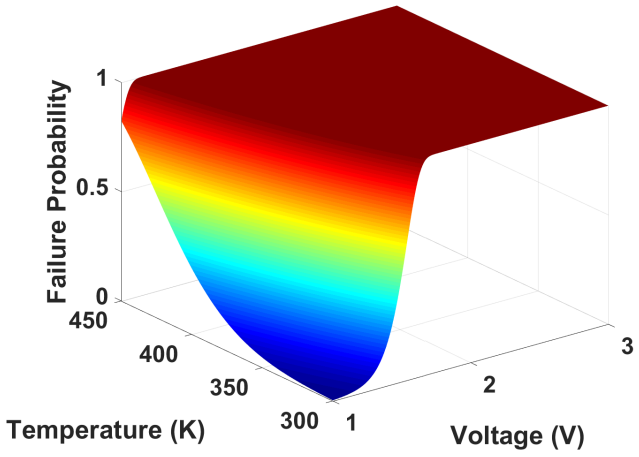
Figure 5.11: Selectivity of the receiver system in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

5.2.2 Total Errors in Estimating Characteristic Lifetime

Using Eqs. (5.2) and (5.3) we can find the lower and upper limit of the selectivity corresponding to the target wearout mechanism. When applying Eq. (5.4), we need to be careful to preprocess the data, since we cannot have any term in the logarithm where it's value is less than or equal to zero. Thus, when using of Eq. (5.4), we can only have variation where selectivity is high enough. This will help in accelerated life test, since one would like to



(a)



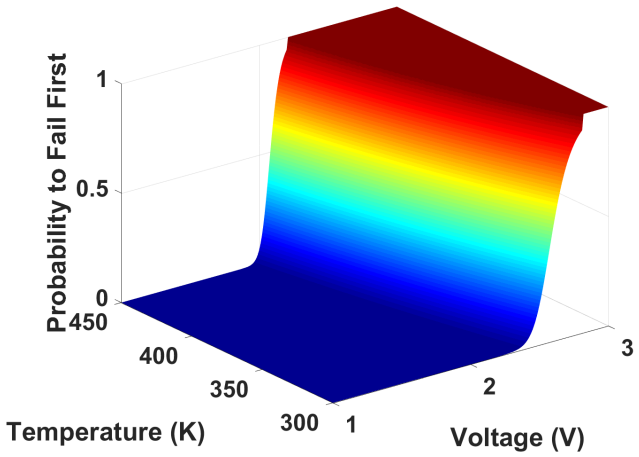
(b)

Figure 5.12: Failure probability of ring oscillator in FinFET technology (a) GOBD and (b) MOL TDDB.

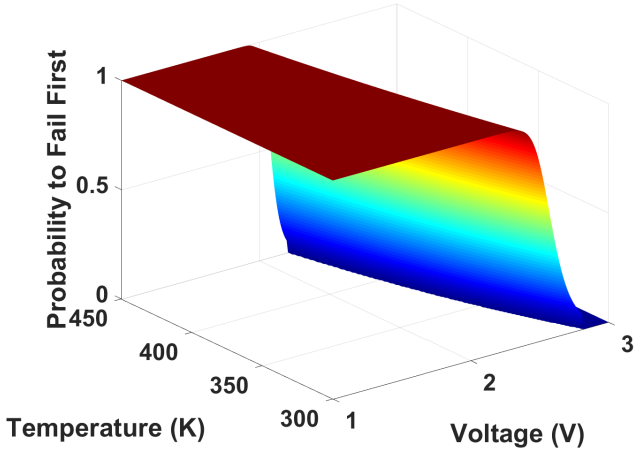
test until observing a large portion of the circuits fail under the specified accelerated test condition.

By using Eq. (5.5), we can obtain the total estimation errors for the ring oscillator, the FFT circuit and the Leon3 microprocessor are shown in Figs. 5.18 to 5.23,. There are logarithmic calculation in Eq. (5.4), and if the value inside a logarithmic calculation is not defined, the function is out of scope. We only keep the results which have mathematical meaning.

For ring oscillator in bulk CMOS technology, the total error for GOBD and MOL



(a)

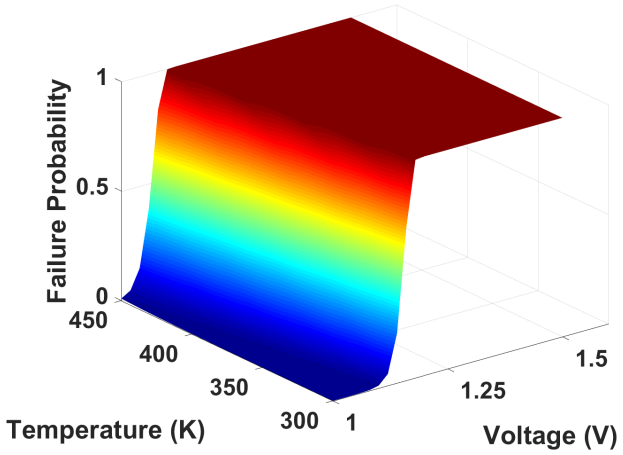


(b)

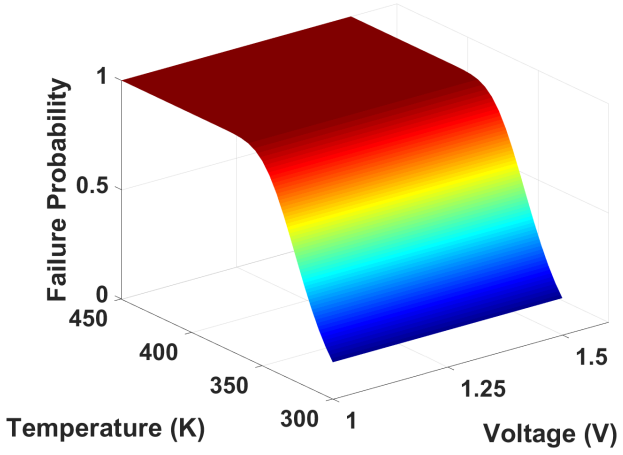
Figure 5.13: Selectivity of the ring oscillator in FinFET technology (a) GOBD and (b) MOL TDDB.

TDDB are shown in Fig. 5.18. we can find that only in high voltage domain the error is defined. For MOL TDDB, only in high temperature domain, we can define the total error.

As for the 8-bit FFT circuit implemented in bulk CMOS technology, after examining Fig. 5.19, we can find that it is not always good to test at the highest voltage and temperature, since at the extreme condition, both GOBD and MOL TDDB will fail, and it is impossible to distinguish them. So it is better to test at a region that one mechanism is failing at a relatively high rate while the other is not.



(a)

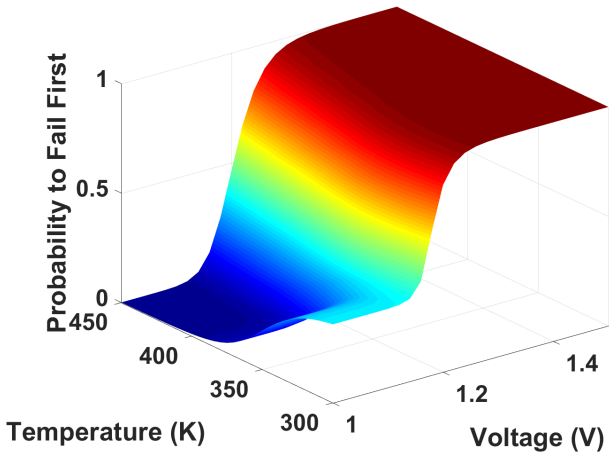


(b)

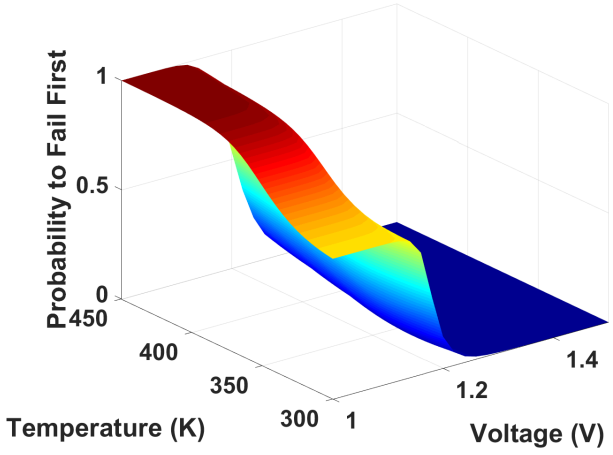
Figure 5.14: Failure probability of the FFT circuit in FinFET technology (a) GOBD and (b) MOL TDDB.

For the receiver system in bulk CMOS technology, the result is quite interesting, as shown in Fig. 5.20. Since the GOBD failure moves up to a higher voltage domain, it gets more possible test regions to test for MOL TDDB. Still, the highest voltage or temperature condition will result in highest error, because of GOBD and MOL TDDB fail at the same time.

In FinFET technology, we expect to obtain lower error in MOL TDDB while get higher error for GOBD. As discussed in previous section, GOBD is not likely to fail at low voltage in FinFET technology while MOL TDDB is more severe.



(a)

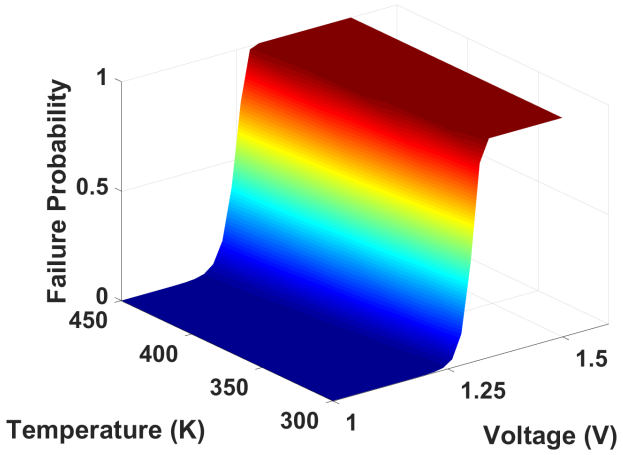


(b)

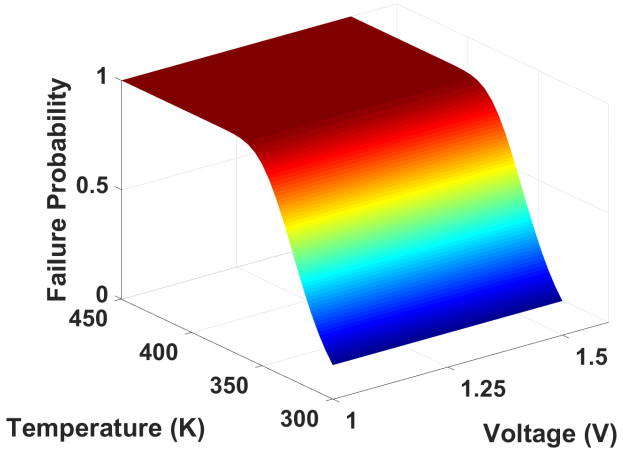
Figure 5.15: Selectivity of the FFT circuit in FinFET technology (a) GOBD and (b) MOL TDDB.

The total estimating errors for GOBD and MOL TDDB for the ring oscillator in FinFET technology can be found in Fig. 5.21. As expected, the total error for estimating GOBD lifetime parameters is higher, shown in Fig. 5.21(a); on the other hand, we can test MOL TDDB relatively easy in low voltage and high temperature domain, depicted in Fig. 5.21(b).

For the FinFET FFT circuit, the total error for estimating GOBD lifetime parameter increases steeply, and we should select the test condition where the error is still small, as shown in the blue region in Fig. 5.22(a). For MOL TDDB, it is better to test at low voltage and high temperature, which verifies the previous claims as well. The total estimating



(a)

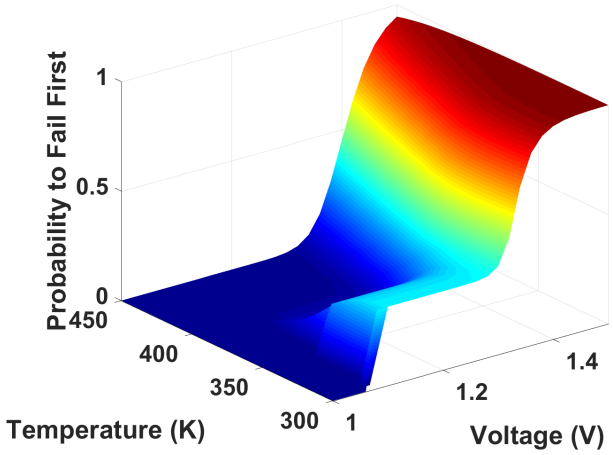


(b)

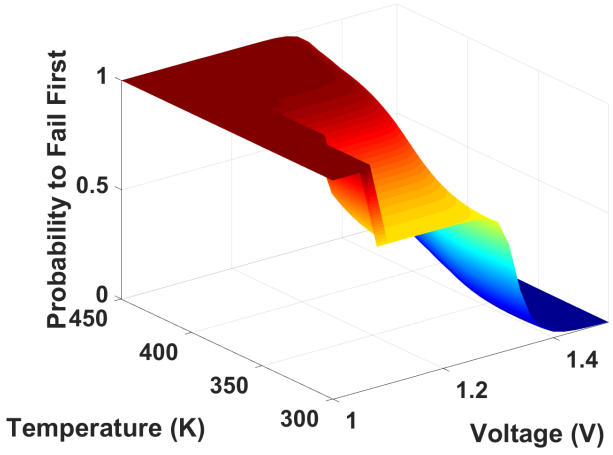
Figure 5.16: Failure probability of the Leon3 microprocessor in FinFET technology (a) GOBD and (b) MOL TDDB.

errors for MOL TDDB is shown in Fig. 5.22(b).

As for the Leon3 microprocessor, since the GOBD fails at a higher voltage, which makes it harder to test GOBD. Shown in Fig. 5.23(a), we can only test GOBD for lower error at some limited domain, while in Fig. 5.23(b), we can have more available region for MOL TDDB.



(a)



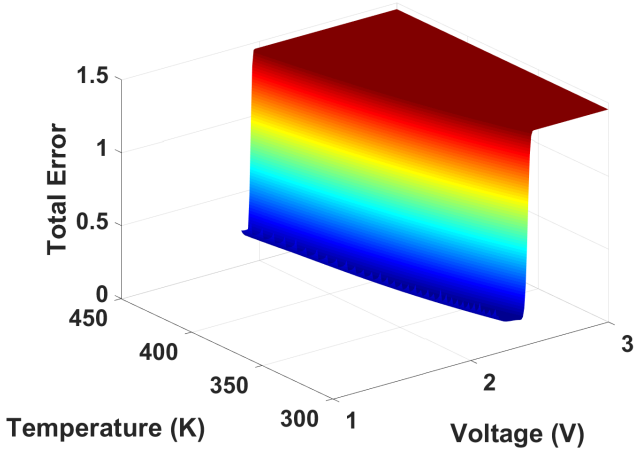
(b)

Figure 5.17: Selectivity of the Leon3 microprocessor in FinFET technology (a) GOBD and (b) MOL TDDB.

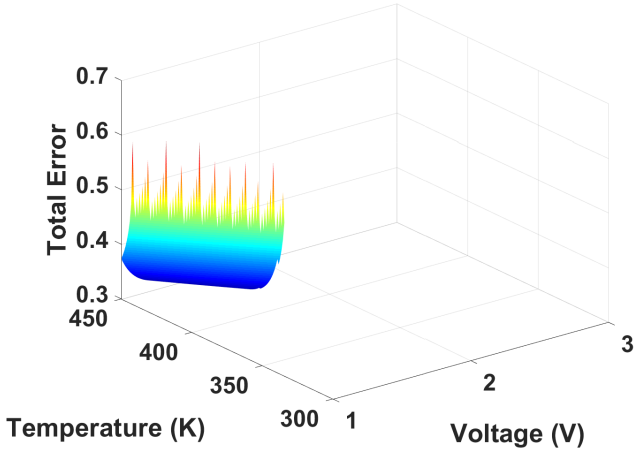
5.2.3 Optimal Test Region

We set the threshold to select the optimal test region where the total estimating errors are less than two times the global minimum errors for each mechanism. With this criterion, we have the optimal test region for FEOL and MOL TDDB for our circuits shown in Figs. 5.24 to 5.29,

For ring oscillator's optimal test region in bulk CMOS technology, we can see the result in Fig. 5.24; we can test MOL TDDB for lower error at relatively high temperature and low



(a)



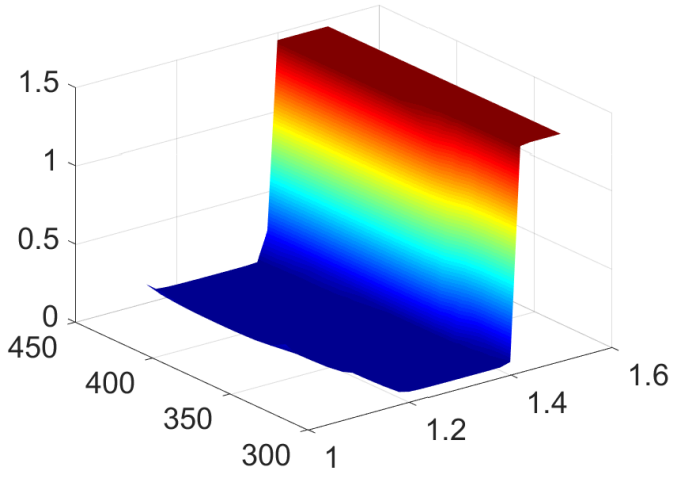
(b)

Figure 5.18: Total estimating errors of the ring oscillator in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

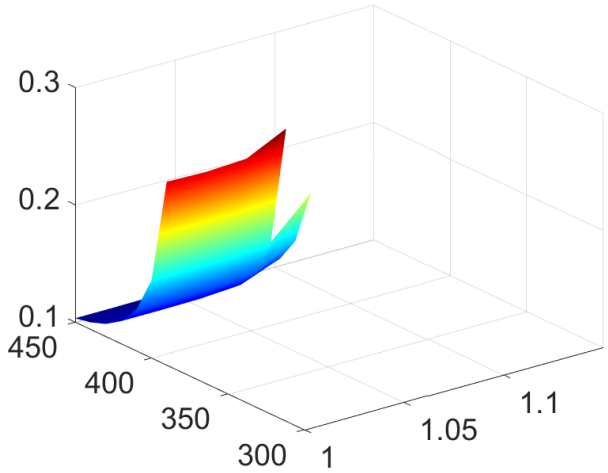
voltage, while testing for GOBD at high voltage, where GOBD fails first.

For the FFT circuit in bulk CMOS technology, since GOBD starts to fail at a lower voltage, it is relatively easy to test for GOBD (larger test region). Since MOL TDDB is not dominant in FinFET technology, we expect to test MOL TDDB at lower voltage but higher temperature domain, as shown in Fig. 5.25.

The layout of the receiver system in bulk CMOS technology is done by hands (more vulnerable features), and thus, the MOL TDDB shows larger test region. Also, in analog circuit, not all the transistors experience the full swing of the supply, thus, the optimal test



(a)



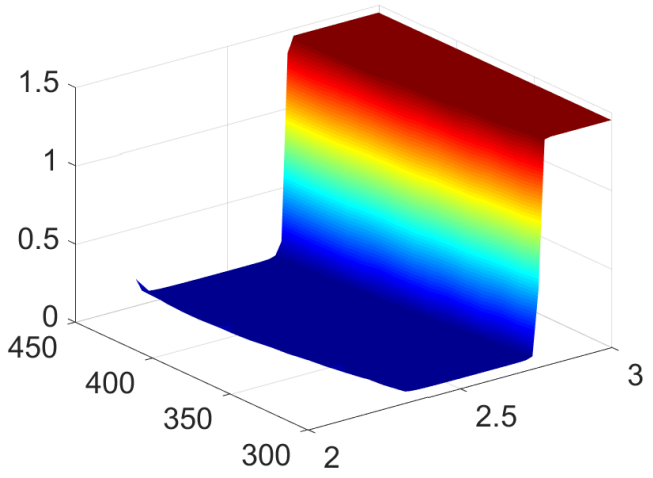
(b)

Figure 5.19: Total estimating errors of the FFT circuit in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

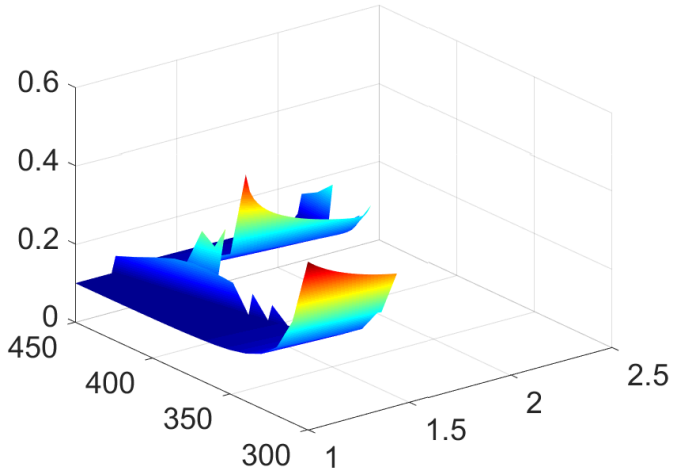
region for GOBD is relatively small. The optimal test region for MOL TDDB and GOBD can be found in Fig. 5.26.

For FinFET technology, we expect to test MOL TDDB easier. For the ring oscillator, the optimal test domain is shown in Fig. 5.27. Since MOL TDDB is more sensitive in FinFET technology, we do find more available for MOL TDDB.

However, as the number of standard cells increasing, it is harder to distinguish GOBD and MOL TDDB, since they both fail at a lower voltage and temperature. So we can only



(a)



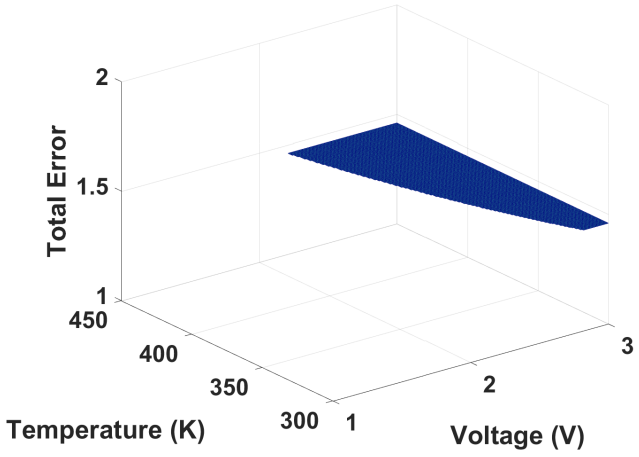
(b)

Figure 5.20: Total estimating errors of the receiver system in bulk CMOS technology (a) GOBD and (b) MOL TDDB.

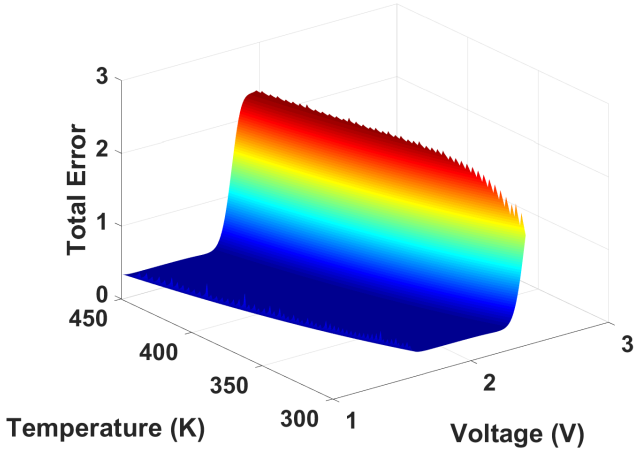
find a small portion of test area to test for the two wearout mechanisms in Fig. 5.28.

The selectivity also depends on the types of standard cells used in the design. For the Leon3 microprocessor, we can find that there is a larger test region for MOL TDDB in Fig. 5.29 at higher temperature, since different standard cells have different vulnerable area and result in different MOL TDDB lifetimes.

To conclude, MOL TDDB is more sensitive to temperature, and we could obtain lower estimation errors for the characteristic lifetime in the high temperature domain. FEOL



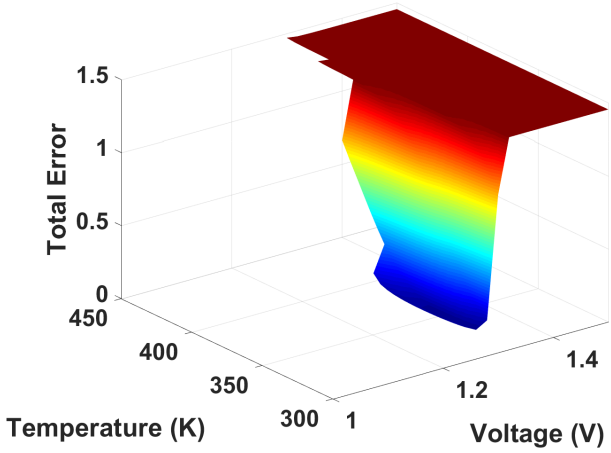
(a)



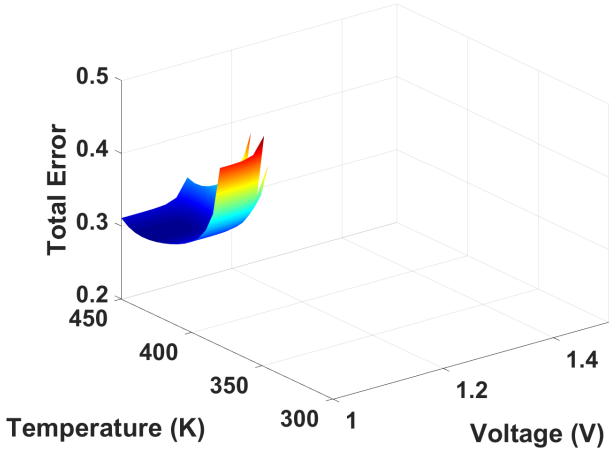
(b)

Figure 5.21: Total estimating errors of the ring oscillator in FinFET technology (a) GOBD and (b) MOL TDDB.

TDDB is more vulnerable under high voltages, and we could get lower estimation errors under higher voltages. However, the specific optimal test domains depend on the type of circuit as well as the size of the circuit. The ring oscillator only has 101 stages which means it needs higher stress to observe a failure, while the large cell count for the FFT circuit and the Leon3 microprocessor make them more likely to fail under accelerated test.



(a)

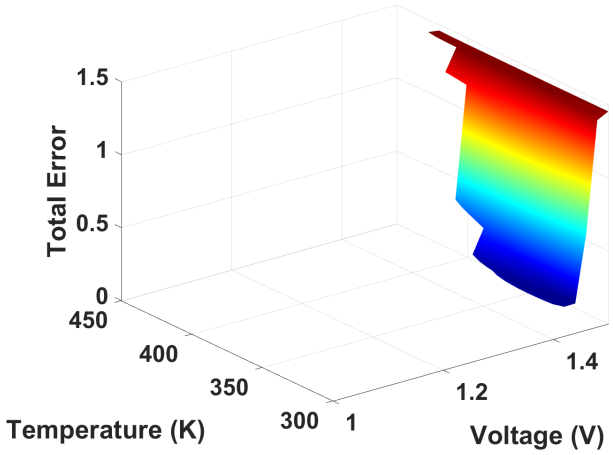


(b)

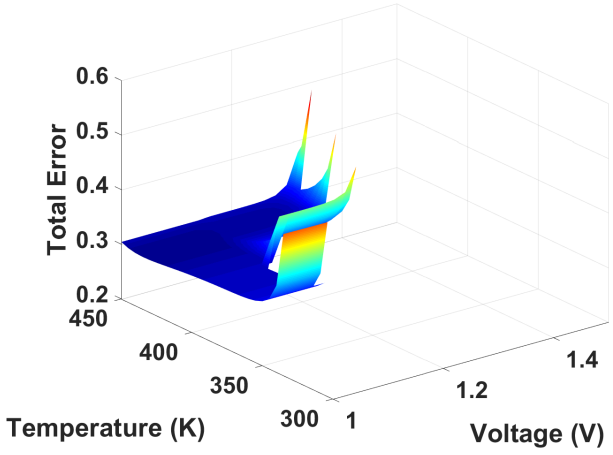
Figure 5.22: Total estimating errors of the FFT circuit in FinFET technology (a) GOBD and (b) MOL TDDB.

5.3 Conclusion

In this chapter, not only the traditional reliability concern, FEOL TDDB is investigated, but also the newly emerging wearout mechanism, MOL TDDB is discussed in detail. The detailed error estimating methodology is introduced and the corresponding optimal accelerated test conditions for these wearout mechanisms are presented. To perform circuit-level accelerated life test, the optimal test conditions vary from circuit to circuit and need to be carefully assessed before conducting the test. Only the test in the optimal region will be



(a)



(b)

Figure 5.23: Total estimating errors of the Leon3 microprocessorin FinFET technology (a) GOBD and (b) MOL TDDB.

able to reflect the target wearout mechanism and degradation, enabling the construction of a model based on circuit failure data. With the accurate device-level wearout model parameters, a circuit designer can use the information to identify the dominant wearout mechanisms under the normal operation conditions and design the circuit in a more robust and reliable fashion.

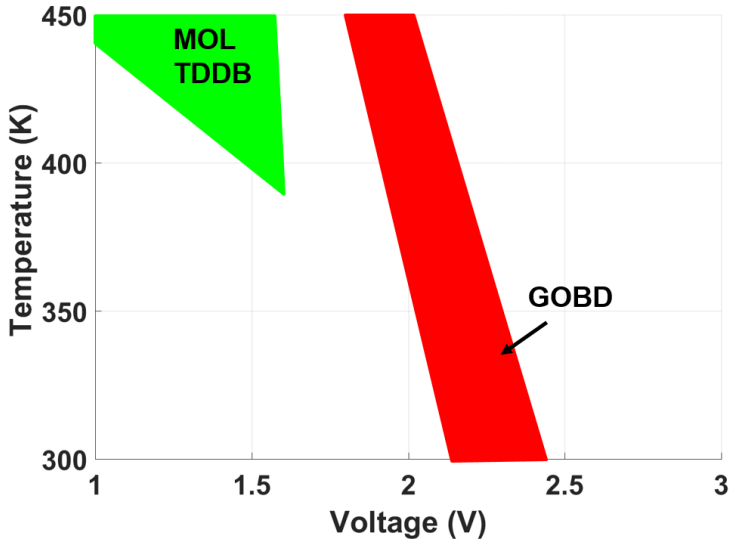


Figure 5.24: Combined domain for detectability and selectivity for the ring oscillator in bulk CMOS technology.

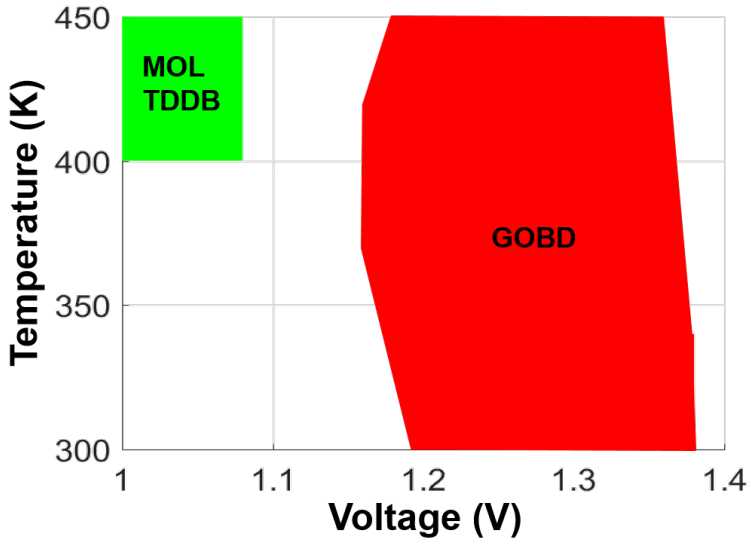


Figure 5.25: Combined domain for detectability and selectivity for the FFT circuit in bulk CMOS technology.

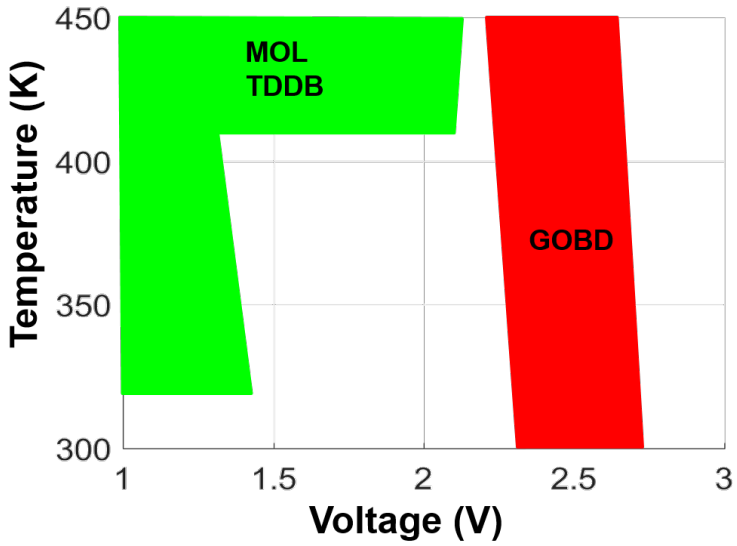


Figure 5.26: Combined domain for detectability and selectivity for the receiver system in bulk CMOS technology.

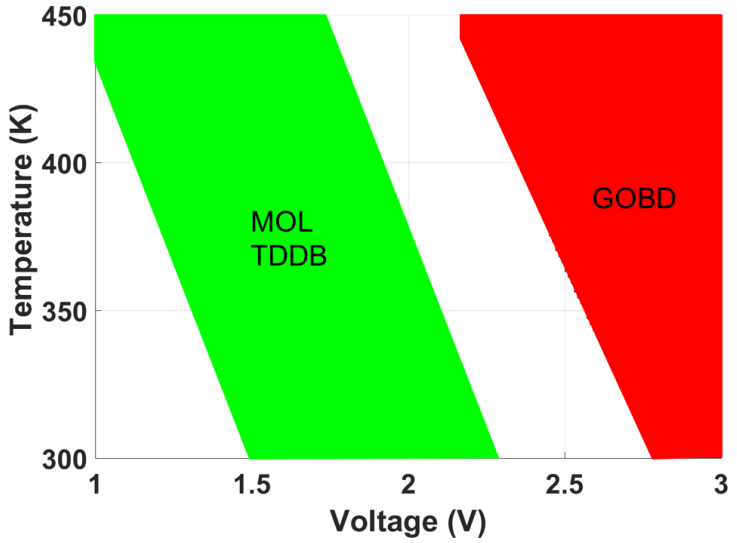


Figure 5.27: Combined domain for detectability and selectivity for the ring oscillator in FinFET technology.

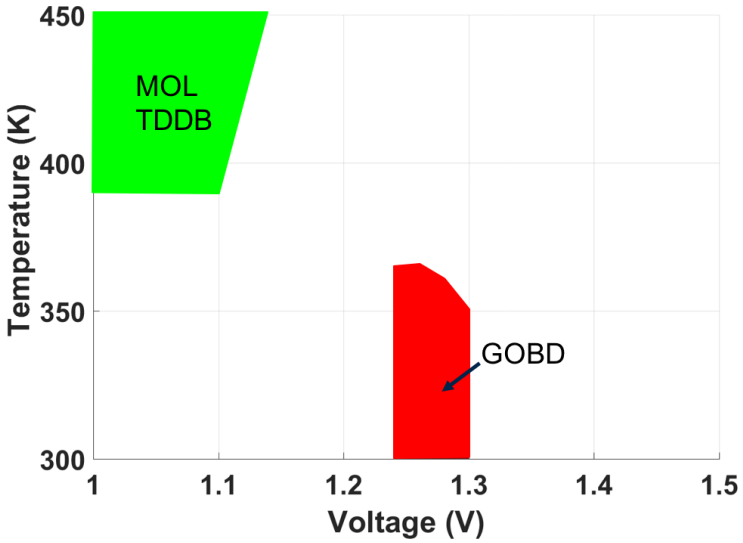


Figure 5.28: Combined domain for detectability and selectivity for the FFT circuit in FinFET technology.

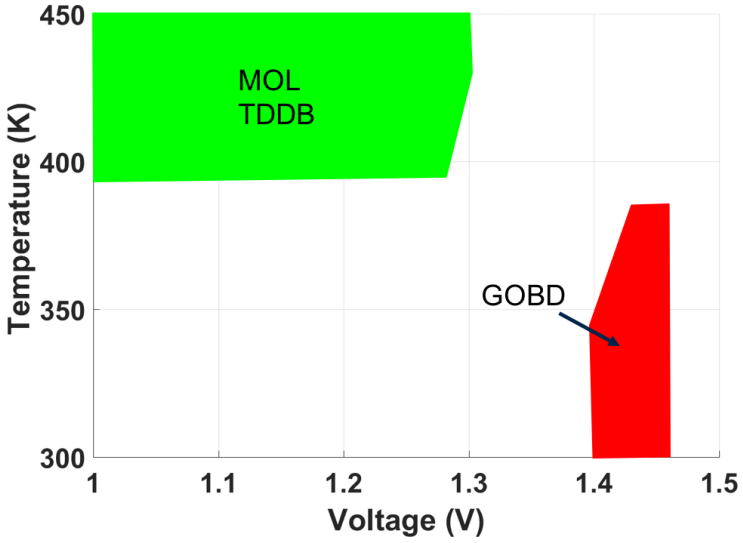


Figure 5.29: Combined domain for detectability and selectivity for the Leon3 microprocessor in FinFET technology.

CHAPTER 6

FRAMEWORK FOR ANALOG CIRCUIT LIFETIME OPTIMIZATION

FEoL failure mechanisms in analog/RF circuit include hot carrier injection (HCI), bias temperature instability (BTI) and TDDB. In analog circuit operation, a large portion of the transistors are operated in continuous mode rather than switching on and off [13].

This chapter presents a FEoL TDDB lifetime and power sensitive design framework to help designers to assess the impact of design parameters, such as transistor width and length. A receiver is taken as an example to illustrate the functionality of our framework.

A novel methodology to link device level FEoL TDDB to circuit performance metrics and power consumption is introduced. By utilizing Monte Carlo simulation, we obtain various sets of performance and lifetime data and we feed the data to MARS to build our predictive model. With the built-up model, we can generate our candidate solutions in the model space and use predefined constraints to find our optimal design strategy. Our framework will help a designer to gain a better understanding about performance, power and lifetime tradeoff before committing to their design to manufacturing, enabling the maximization of power and lifetime.

6.1 MARS

MARS (multivariate adaptive regression splines) is a form of regression analysis introduced by Jeremo H.Friedman in 1991 [105]. It is an adaptive procedure for multivariate nonparametric regression. That is, it doesn't take a predetermined form, but it constructs the model structure according to the information derived from the data.

MARS technique is well suited for high-dimensional problems while capturing essential nonlinearities and interactions. Due to its adaptive nature, MARS can "filter out" the negligible parameters without manual intervention. MARS can automatically capture es-

sential parameters while removing negligible parameters through its intelligent process.

MARS builds models of the form:

$$\hat{f}(x) = \sum_{i=1}^{k} c_i B_i(x) \tag{6.1}$$

The model is a weighted sum of basis functions $B_i(x)$, which is either a constant 1, a hinge function or a product of two or more hinge functions. Each c_i is a constant coefficient.

A hinge function is the form of $(x-t)_+$ or $(t-x)_+$ which are defined as:

$$(x-t)_+ = \begin{cases} x-t, & \text{if } x > t, \\ 0, & \text{otherwise}, \end{cases} \tag{6.2}$$

$$(t-x)_+ = \begin{cases} t-x, & \text{if } x < t, \\ 0, & \text{otherwise}, \end{cases} \tag{6.3}$$

In MARS, Eqs. (6.2) and (6.3) are called a reflected pair, shown in Fig. 6.1(a). MARS uses reflected pairs of hinge function for each X_j with knots at each observed value x_{ij}; an example is shown in Fig. 6.1(b).

There are 3 step in MARS model building process: the forward pass, the backward pass and the generalized cross validation.

In the forward pass, MARS starts with a model which consists of just the intercept term (the mean of the response values). It repeatedly adds basis function in pairs to the model. In each step, it finds the pair that gives the maximum reduction in residual sum-of-squares (a greedy method). The two basis functions are identical except that a different side of a mirrored hinge function is used for each function. Each new basis function consists of a term already in the model (which could perhaps be the intercept term) multiplied by a new hinge function.

To add a new basis function, MARS searches over all combination of the follows: ex-

isting terms, all variables (to select one for the new basis function) and all values of each variable (for the knot of the new hinge function). To calculate the coefficient of each term, MARS applies a linear regression over the terms. This process continues until the change in residual error is small enough or maximum number of term is reached.

In the backward pass, since the forward pass usually builds an over-fit model (no generalization), the backward pass prunes the model by removing the least effective terms one by one, until it finds the best sub-model. Also, all the model subsets are compared using the GCV (generalized cross validation) criterion. Although the forward pass adds terms in pairs, the backward pass discards one side of the pair.

For the generalized cross validation phase, the equation for GCV is shown as follow,

$$GCV = \frac{RSS}{N * (1 - \frac{EPN}{N})^2} \tag{6.4}$$

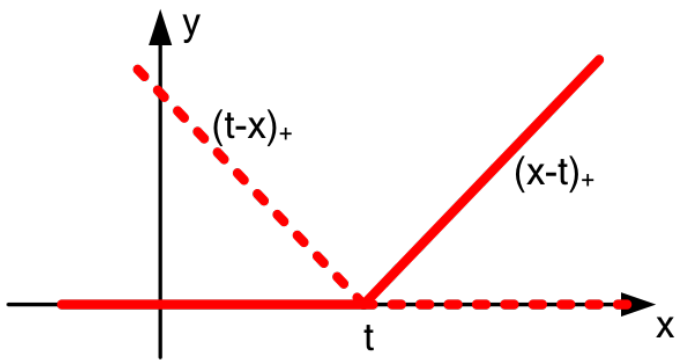
where RSS is the residual sum-of-squares, N is the number of observations, EPN is the effective parameters number.

In our paper, we use circuit simulation results to build a regression model through MARS; and use this model to help us find the optimal design region.

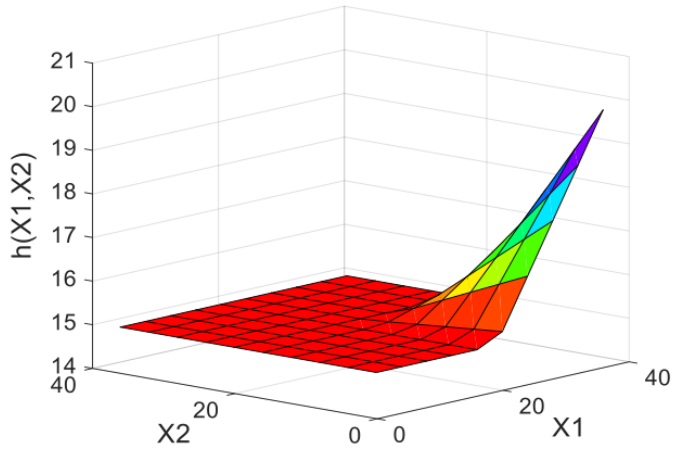
6.2 Circuit Performance And Lifetime Assessment

The receiver circuit is widely deployed in all sorts of radio frequency (RF) systems nowadays. A typical receiver system is shown in Fig. 5.4(a). In this study, only the analog part of the receiver system (shown in the dashed square in Fig. 5.4(a)) is considered. Shown in Fig. 5.4(b) and (c), an active-feedback LNA and a classic Gilbert Cell mixer are implemented with the IBM 90nm process.

In this study, we use Cadence Virtuoso to perform circuit performance simulation. The performance metrics include gain, 1dB compression point (P1dB), input referred third-order intercept point (IIP3), noise figure (NF) and input matching (S11). We also consider



(a)



(b)

Figure 6.1: Explanation of MARS (a) a pair of hinge functions with a knot at t (b) using MARS to model nonlinearity.

power consumption of the receiver.

In RFIC design, designers keep the minimum device length to get the maximum f_t (cut-off frequency) and f_{max} (maximum oscillation frequency); and thus, we focus on optimize device width in this paper. By running Monte Carlo simulations, we get multiple sets of data; each set consists of different device widths and the corresponding circuit performance.

The flow chart of our framework is shown in Fig. 6.2. We first perform Monte Carlo simulations on the target receiver system to get performance and power consumption. We keep track of each device size and its gate source voltage for lifetime calculation. For each transistor in the receiver system, we use Eq. (3.1) together with the transistor gate

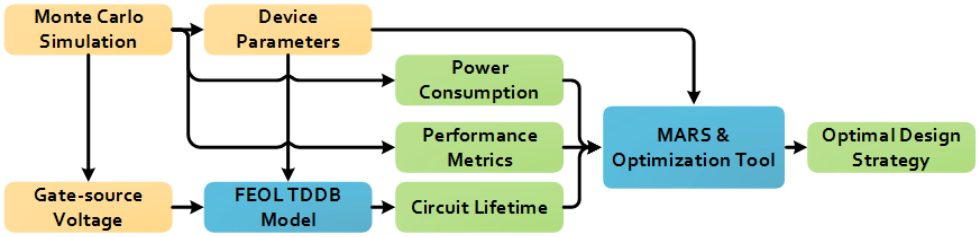


Figure 6.2: Framework of power and lifetime sensitive optimization system. The MARS model is built on data which are generated through Monte Carlo simulation.

voltage and size information to calculate its characteristic lifetime. Then we use Eqs. (3.3) to (3.5) to get the total lifetime of the receiver system. With the performance metrics and lifetime result, we feed these data to MARS to generate our prediction model for future optimization. The detailed optimization process is introduced in the next section.

To verify that MARS gives us the accurate model, we use the same width information used for simulation to check its accuracy. The average relative error is 2.43%.

6.3 Circuit Optimization

After building the model in MARS, we can sweep any of the design parameters to check their impacts on performance metrics, power and lifetime. In Fig. 6.3, we sweep the width of M_{RF} in the mixer to see its impact on performance. The red dotted line represents the design constraints. Fig. 6.4 shows the power and lifetime relationship with the width of M_{RF}. Combined with these two, we can conclude that we would like to have a narrower M_{RF} for lower power and longer lifetime; however, the performance metrics prevent us from doing so. The specifications of P1dB, IIP3 and noise figure will be violated with a narrower M_{RF}.

In addition, our model can determine the significant factors that influence the circuit performance. Shown in Figs. 6.5 and 6.6, we run the sweep of M_{sw}, we find that the performance will not change much with the width of M_{sw}. This can be verified by inspecting the circuit. As we can see in the mixer circuit, M_{sw} are the switching transistors. If M_{sw1}-M_{sw4} perform the switching function correctly, the circuit will remain functional and will

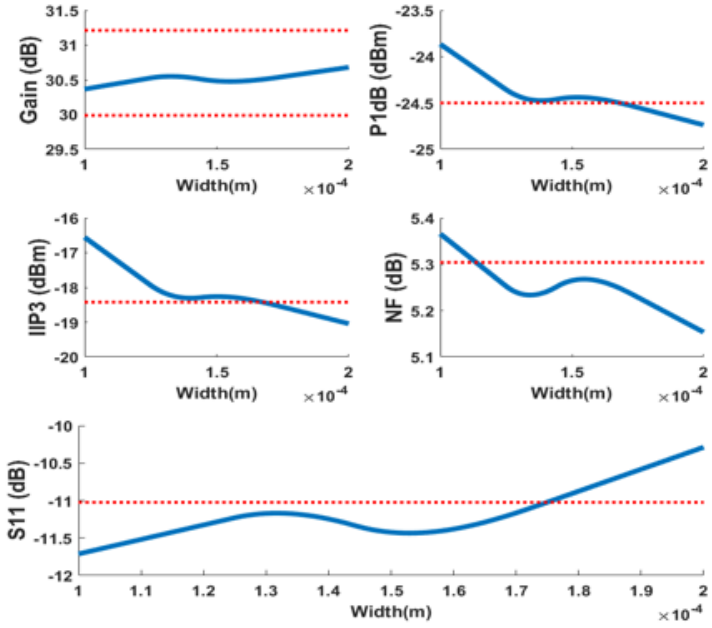
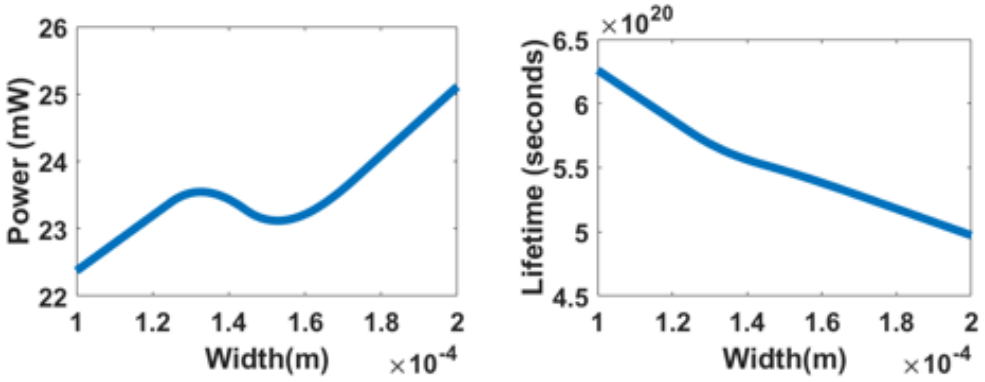


Figure 6.3: Receiver performance metrics vs M_{RF}'s width. The red dotted line represents performance bound for each metric.



(a) (b)

Figure 6.4: Receiver (a) power consumption vs M_{RF}'s width and (b) lifetime vs M_{RF}'s width.

not have a big impact on performance. On the contrary, the input transistor M_{sw} determines the performance of the mixer, since it is the key transistor providing the gain and input matching.

To better regularize our optimization process, we define a performance score (PS) for each performance metric to quantify how far our performance metrics can be from our

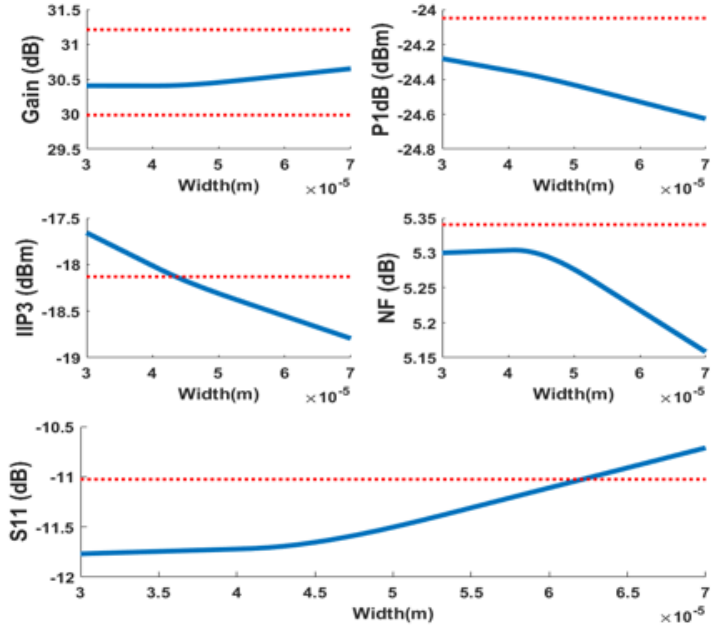
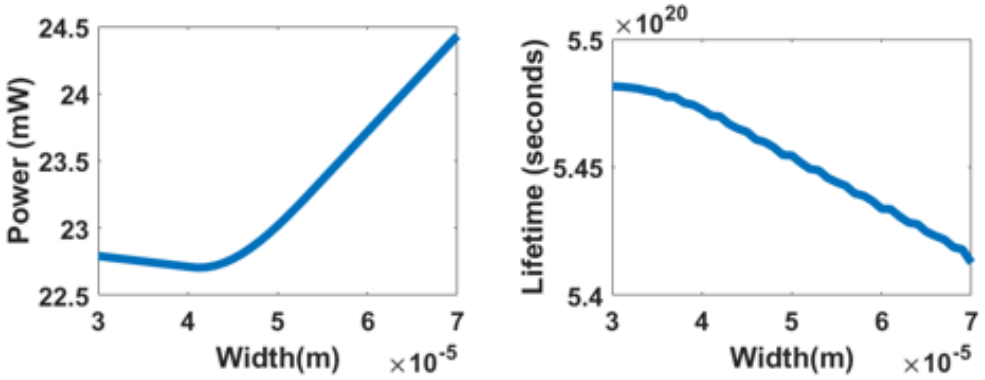


Figure 6.5: Receiver performance metrics vs M_{sw}'s width. The red dotted line represents the performance bound for each metric.



(a) (b)

Figure 6.6: Receiver (a) power consumption vs M_{sw}'s width and (b) lifetime vs M_{sw}'s width.

specification,

$$PS = A \cdot \left| \frac{X}{X_{spec}} \times 100\% - (100 - \delta_x) \right|^2 \tag{6.5}$$

where X stands for the performance metrics, i.e. gain, P1dB, IIP3, NF, power, lifetime;

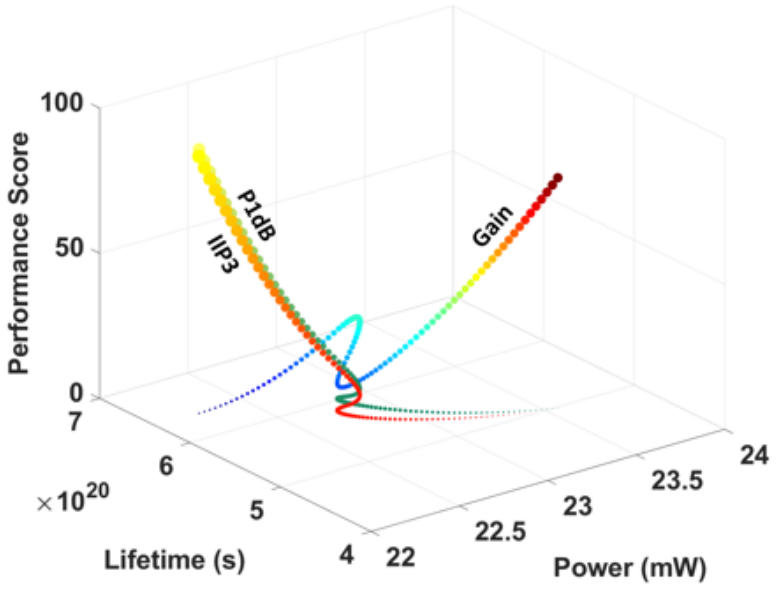
X_{spec} is the specified performance metric value before optimization, ffi_X is the maximum percentage shift in performance. δ_X can be either positive or negative; it depends on whether the higher or lower the metric is better. For example, the higher gain is better; and thus, δ_X is positive for gain. A is a scale factor to normalized the performance score in the range [0, 100].

Fig. 6.7 presents the power, lifetime and performance metrics trade-off when tuning the width of M_{RF}. Fig. 6.7(a) presents the trade-off between gain and linearity (P1dB and IIP3), while Fig. 6.7(b) gives us a sense of how can we choose between gain, noise figure (NF) and input matching (S11). As we can see in Fig. 6.7, as the gain of the receiver system increases, we have better linearity and noise performance but degraded input matching.

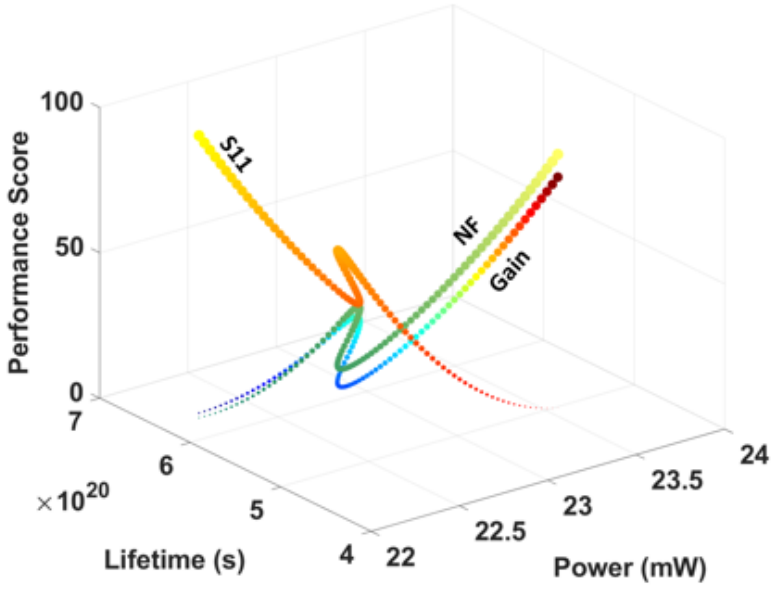
It is impossible to find a best point for every performance metric, not to mention to consider power and circuit lifetime at the same time. However, if we apply some constraints on performance metrics, power and lifetime, we could find an optimal solution for our specific application.

The detailed optimization flow is presented in Fig. 6.8. We first input the performance specification of our receiver. Our simulator will use the calculated MARS model to generate all possible candidates, and the simulator will search in the candidate space to check whether a possible solution can be found, i.e., to check if the specification is in the range of our prediction. If no possible solution can be found, the user should decide whether to alleviate the requirement and perform the search with the new specification again. If an optimal design strategy is found, we will output its performance metrics, power and lifetime with its corresponding sizing information.

Our optimization has multiple modes for the user to select. The first one is to maximize performance; in this mode, our optimization model will search the set of design parameters that result in a maximum total performance score. The second mode is to maximize the lifetime of the circuit; similarly, our framework will produce the design parameters that yield the maximum lifetime possible. The last mode is to minimize power; our framework



(a)



(b)

Figure 6.7: Design trade-off tuning M_{RF}. (a) gain vs linearity (P1dB and IIP3) (b) gain vs noise figure (NF) and input matching (S11).

will produce the set of design parameters that give the minimum power. In all the modes, one can set a minimum requirement on each performance metric. This is implemented to avoid the extreme case where one performance metric yields a high score while others fail

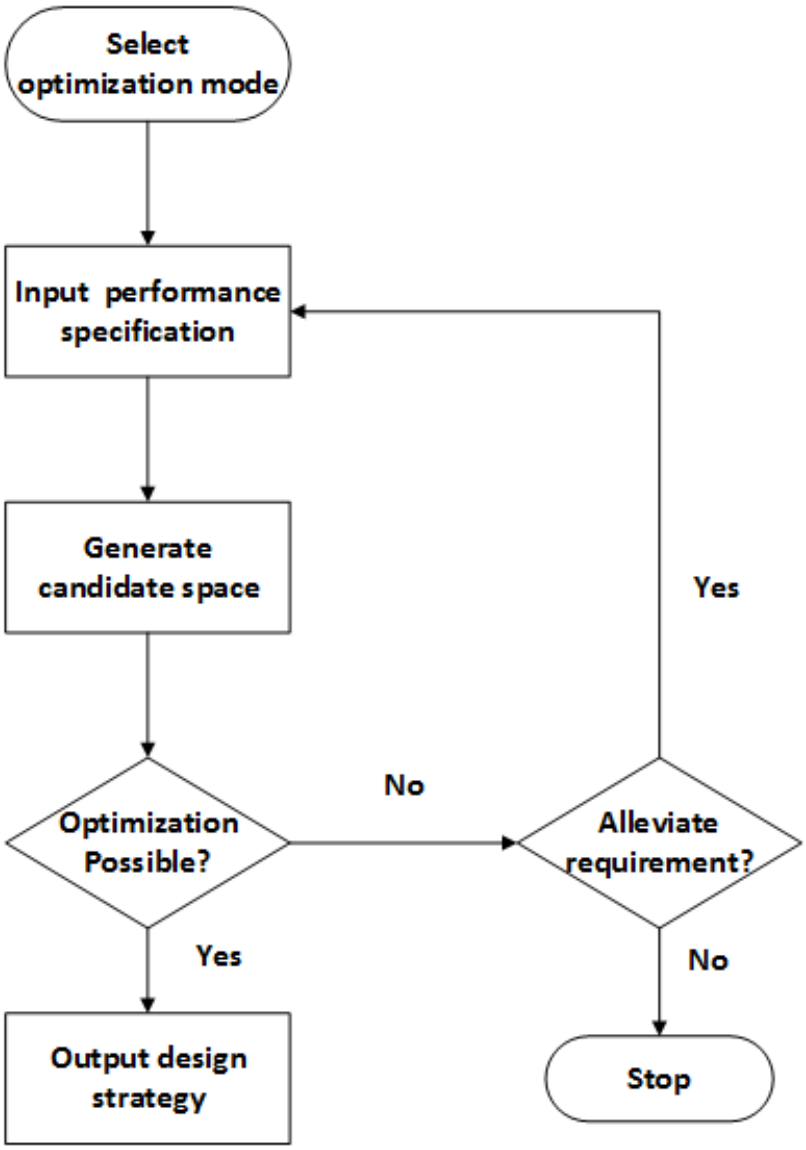


Figure 6.8: Optimization flow.

to meet their specifications.

The optimization result of different optimization modes can be found in Fig. 6.9. The final optimal sizing information of different modes for the receiver is shown in **??**. As we can see in Fig. 6.9, the maximum score mode gives us the total maximum score. However, this might not be the best choice for a circuit designer, since in this mode, one performance metric may dominate the total score. In this example, the IIP3 performance metric seems dominant. Also, the maximum power mode does not save a large amount of power in this

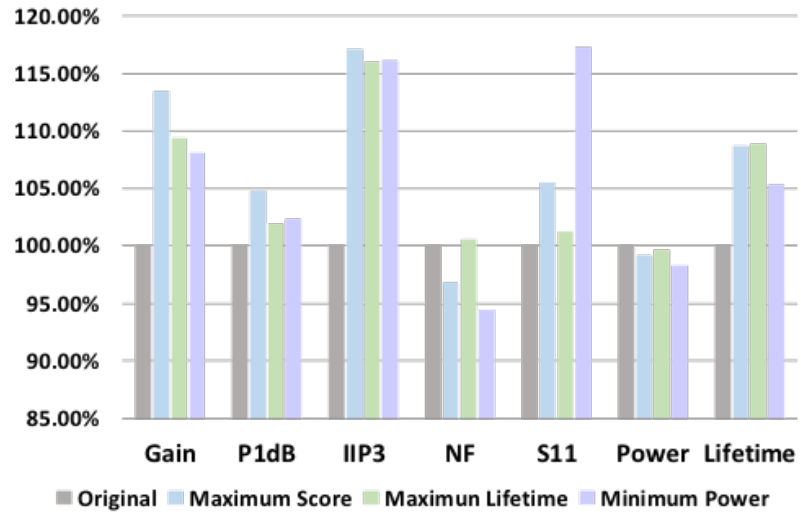


Figure 6.9: Comparison between the original design and the optimal design. The optimal design trades power for lifetime.

Table 6.1: Sizing for Different Optimization Modes

	Original	Max Score	Max Lifetime	Min Power
$M_1(\mu m)$	300	250	250	250
$M_2(\mu m)$	10	10	9	10
$M_{RF}(\mu m)$	150	130	140	140
$M_{SW}(\mu m)$	50	55	45	49

application. This can be explained by the requirements of other performance metrics; that is, if we alleviate the requirement on other performance metrics, a more power saving optimization point can be found. It is always the designer's choice to alleviate some constraints to trade with other more important metrics.

6.4 Conclusion

A novel lifetime sensitive design optimization framework is proposed for FEoL TDDB in this chapter. By utilizing our framework, one can find the trade-off between circuit performance, power and lifetime in a quick and accurate manner. Given the framework, a fully automated design optimization system for lifetime, power and performance metrics

is achieved. Circuit designers can use our framework to identify the critical performance metrics and deal with the circuit power consumption and lifetime concerns at the same time.

CHAPTER 7
CONCLUSION AND FUTURE DIRECTIONS

7.1 Summary of the presented work

This thesis investigates not only the traditional reliability concern, GOBD, but also the newly emerging wearout mechanism, MOL TDDB. A TDDB lifetime simulator for both traditional bulk CMOS and FinFET technology is proposed for the target wearout mechanisms. The shrinking feature size in FinFET technology leads to severe degradation caused by MOL TDDB because of its sensitivity to alignment errors. On the other hand, voltage scaling alleviates the impact of GOBD and MOL TDDB. Process variation is taken into consideration and becomes a significant factor affecting a circuits' lifetime distribution.

With reliability simulation, a circuit designer can use the information to redesign a circuit or to redraw the layout in a more robust and reliable way; also, a circuit designer can use application specific information to choose certain cells that have longer lifetimes than others. It is also possible to use the lifetime information to add some constraints on circuit design to ensure the circuit's performance over the product lifetime.

Manufacturers can utilize the optimal test region to find the best test region for estimating wearout model parameters. Also, they can select the correct region to test for certain wearout mechanism.

A novel lifetime sensitive design optimization framework is proposed for GOBD. By utilizing our framework, one can find the trade-off between circuit performance, power and lifetime in a quick and accurate manner. Given the framework, a fully automated design optimization system for lifetime, power and performance metrics is achieved. Circuit designers can use our framework to identify the critical performance metrics and deal with the circuit power consumption and lifetime concerns at the same time.

7.2 Open questions

Through the studies of GOBD reliability in FinFET technology, the traditional gate oxide hard-breakdown model is implemented. FinFET transistors are treated as planar device in the studies. However, since the geometry of FinFET transistor is different from the traditional bulk CMOS, the electric fields that are not perpendicular to the gate may need to be taken into consideration with more accurate model.

Also, in the fabricated FinFET device, the electric field at the tip of the gate may be orders of magnitude larger than the calculated one. This large electric field may be a factor to accelerate the gate oxide breakdown and may need to be considered in future studies.

In addition, the effects of wearout mechanisms in circuits usually interact with each other. For example, the heating caused by EM may lead to a local hot spot and accelerate other wearout mechanisms. Both GOBD and BTI depend on defects generation, and one may have impacted on the other in real life scenarios, which may need more thorough investigation to incorporate the effects in circuit degradation.

7.3 The future direction

This work gives a framework for optimization for the trade-off between power, area and lifetime in analog circuit; for its digital counterpart, the trade-off between area, power and performance needs further investigation, since optimization in digital circuit involve redesigning of standard cell library.

Also, in this thesis only GOBD and MOL TDDB are considered. Future work can add more wearout mechanisms, such as BTI and HCI in the frontend-of-line, together with the backend-of-line wearout mechanisms: backend TDDB, electromigration (EM) and stress induced voiding (SIV).

In addition, one can use the simulator to generate lots of test data and feed it to some machine learning method to build a framework for circuit's health prediction. That is,

by supply different testvectors for a circuit under different wearout stages, on can build a model mapping performance degradation to transistor degradation; and use that information to know how much degradation the circuit has and how long it can operate in the future.

REFERENCES

[1] Shinji Yokogawa. “Simulation study for lifetime distribution of middle-of-line time-dependent dielectric breakdown affected by global and local spacing variations”. In: *Japanese Journal of Applied Physics* 55.6S3 (2016), 06JF02.

[2] F. Chen, C. Graas, M. Shinosky, C. Griffin, R. Dufresne, R. Bolam, C. Christiansen, Kai Zhao, S. Narasimha, C. Tian, and Choon-Leong Lou. “New breakdown data generation and analytics methodology to address BEOL and mol dielectric TDDB process development and technology qualification challenges”. In: *2014 IEEE International Reliability Physics Symposium*. 2014, 3A.1.1–3A.1.11.

[3] F. Chen, Carole Graas, Michael Shinosky, Kai Zhao, Shreesh Narasimha, Xiao Hu Liu, and Chunyan Tian. “Breakdown data generation and in-die deconvolution methodology to address BEOL and MOL dielectric breakdown challenges”. In: *Microelectronics Reliability* 55.12, Part B (2015), pp. 2727 –2747.

[4] E. Wu, J. Stathis, B. Li, B. Linder, K. Zhao, and G. Bonilla. “A critical analysis of sampling-based reconstruction methodology for dielectric breakdown systems (BEOL/MOL/FEOL)”. In: *2015 IEEE International Reliability Physics Symposium*. 2015, 2A.2.1–2A.2.11.

[5] X. Federspiel, D. Nouguier, D. Ney, and T. Ya. “Conductivity and reliability of 28nm FDSOI middle of the line dielectrics”. In: *2017 IEEE International Reliability Physics Symposium (IRPS)*. 2017, DG–9.1–DG–9.4.

[6] Ernest Y. Wu, Ronald Bolam, Ronald Filippi, James H. Stathis, Baozhen Li, and Andrew Kim. “Applications of clustering model to bimodal distributions for dielectric breakdown”. In: *Journal of Vacuum Science & Technology B* 35.1 (2017), 01A112. eprint: `https://doi.org/10.1116/1.4972871`.

[7] P. J. Roussel, A. Chasin, S. Demuynck, N. Horiguchi, D. Linten, and A. Mocuta. “New methodology for modelling MOL TDDB coping with variability”. In: *2018 IEEE International Reliability Physics Symposium (IRPS)*. 2018, 3A.5–1–3A.5–6.

[8] T. Shen, K. B. Yeap, C. Christiansen, and P. Justison. “Field acceleration factor extraction in MOL and BEOL TDDB”. In: *2017 IEEE International Reliability Physics Symposium (IRPS)*. 2017, DG–2.1–DG–2.5.

[9] Y. C. Ong, S. C. Lee, and A. S. Oates. “Percolation defect nucleation and growth as a description of the statistics of electrical breakdown for gate, MOL and BEOL

dielectrics". In: *2018 IEEE International Reliability Physics Symposium (IRPS)*. 2018, P–GD.7–1–P–GD.7–6.

[10] I.M. Mackintosh. "The reliability of integrated circuits". In: *Microelectronics Reliability* 5.1 (1966), pp. 27 –37.

[11] Taizhi Liu, Chang-Chih Chen, Woongrae Kim, and Linda Milor. "Comprehensive reliability and aging analysis on SRAMs within microprocessor systems". In: *Microelectronics Reliability* 55.9 (2015). Proceedings of the 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, pp. 1290 –1296.

[12] R. Zhang, T. Liu, K. Yang, and L. Milor. "Modeling for SRAM reliability degradation due to gate oxide breakdown with a compact current model". In: *2017 32nd Conference on Design of Circuits and Integrated Systems (DCIS)*. 2017, pp. 1–5.

[13] K. Yang, T. Liu, R. Zhang, and L. Milor. "A lifetime and power sensitive design optimization framework for a radio frequency circuit". In: *2017 IEEE International Integrated Reliability Workshop (IIRW)*. 2017, pp. 1–4.

[14] J. W. Bandler and S. H. Chen. "Circuit optimization: the state of the art". In: *IEEE Transactions on Microwave Theory and Techniques* 36.2 (1988), pp. 424–443.

[15] J. H. Stathis. "Percolation models for gate oxide breakdown". In: *Journal of Applied Physics* 86.10 (1999), pp. 5757–5766. eprint: `https://doi.org/10.1063/1.371590`.

[16] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, and G. Groeseneken. "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability". In: *IEEE Transactions on Electron Devices* 49.3 (2002), pp. 500–506.

[17] M. Depas, M. M. Heyns, and P. W. Mertens. "Soft Breakdown of Ultra-Thin Gate Oxide Layers". In: *ESSDERC '95: Proceedings of the 25th European Solid State Device Research Conference*. 1995, pp. 235–238.

[18] S. Holland, I. C. Chen, T. P. Ma, and C. Hu. "On physical models for gate oxide breakdown". In: *IEEE Electron Device Letters* 5.8 (1984), pp. 302–305.

[19] B. Kaczer, R. Degraeve, A. De Keersgieter, K. Van de Mieroop, V. Simons, and G. Groeseneken. "Consistent model for short-channel nMOSFET after hard gate oxide breakdown". In: *IEEE Transactions on Electron Devices* 49.3 (2002), pp. 507–513.

[20] E. Takeda and N. Suzuki. "An empirical model for device degradation due to hot-carrier injection". In: *IEEE Electron Device Letters* 4.4 (1983), pp. 111–113.

[21] E. Takeda, A. Shimizu, and T. Hagiwara. “Role of hot-hole injection in hot-carrier effects and the small degraded channel region in MOSFET’s”. In: *IEEE Electron Device Letters* 4.9 (1983), pp. 329–331.

[22] E. Takeda, Y. Nakagome, H. Kume, and S. Asai. “New hot-carrier injection and device degradation in submicron MOSFETs”. In: *IEE Proceedings I (Solid-State and Electron Devices)* 130 (3 1983), 144–150(6).

[23] W. Weber. “Dynamic stress experiments for understanding hot-carrier degradation phenomena”. In: *IEEE Transactions on Electron Devices* 35.9 (1988), pp. 1476–1486.

[24] E. Rosenbaum, R. Rofan, and C. Hu. “Effect of hot-carrier injection on n- and pMOSFET gate oxide integrity”. In: *IEEE Electron Device Letters* 12.11 (1991), pp. 599–601.

[25] Dieter K. Schroder and Jeff A. Babcock. “Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing”. In: *Journal of Applied Physics* 94.1 (2003), pp. 1–18. eprint: `https://doi.org/10.1063/1.1567461`.

[26] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder. “Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultra Fast VT-Measurements”. In: *2006 IEEE International Reliability Physics Symposium Proceedings*. 2006, pp. 448–453.

[27] Dieter K. Schroder. “Negative bias temperature instability: What do we understand?” In: *Microelectronics Reliability* 47.6 (2007). Modelling the Negative Bias Temperature Instability, pp. 841 –852.

[28] H. Reisinger, T. Grasser, W. Gustin, and C. Schlünder. “The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress”. In: *2010 IEEE International Reliability Physics Symposium*. 2010, pp. 7–15.

[29] P. M. Lenahan, J. P. Campbell, A. T. Krishnan, and S. Krishnan. “A Model for NBTI in Nitrided Oxide MOSFETs Which Does Not Involve Hydrogen or Diffusion”. In: *IEEE Transactions on Device and Materials Reliability* 11.2 (2011), pp. 219–226.

[30] V. Huard, M. Denais, and C. Parthasarathy. “NBTI degradation: From physical mechanisms to modelling”. In: *Microelectronics Reliability* 46.1 (2006), pp. 1 –23.

[31] R.J.O.M. Hoofman, G.J.A.M. Verheijden, J. Michelon, F. Iacopi, Y. Travaly, M.R. Baklanov, Zs. Tökei, and G.P. Beyer. “Challenges in the implementation of low-

k dielectrics in the back-end of line". In: *Microelectronic Engineering* 80 (2005). 14th biennial Conference on Insulating Films on Semiconductors, pp. 337 –344.

[32] R. Tsu, J. W. McPherson, and W. R. McKee. "Leakage and breakdown reliability issues associated with low-k dielectrics in a dual-damascene Cu process". In: *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059)*. 2000, pp. 348–353.

[33] J. Noguchi, T. Saito, N. Ohashi, H. Ashihara, H. Maruyama, M. Kubo, H. Yamaguchi, D. Ryuzaki, K. . Takeda, and K. Hinode. "Impact of low-k dielectrics and barrier metals on TDDB lifetime of Cu interconnects". In: *2001 IEEE International Reliability Physics Symposium Proceedings. 39th Annual (Cat. No.00CH37167)*. 2001, pp. 355–359.

[34] E. T. Ogawa, Jinyoung Kim, G. S. Haase, H. C. Mogul, and J. W. McPherson. "Leakage, breakdown, and TDDB characteristics of porous low-k silica-based interconnect dielectrics". In: *2003 IEEE International Reliability Physics Symposium Proceedings, 2003. 41st Annual.* 2003, pp. 166–172.

[35] G. S. Haase, E. T. Ogawa, and J. W. McPherson. "Breakdown characteristics of interconnect dielectrics". In: *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.* 2005, pp. 466–473.

[36] J. W. McPherson. "Determination of the nature of molecular bonding in silica from time-dependent dielectric breakdown data". In: *Journal of Applied Physics* 95.12 (2004), pp. 8101–8109. eprint: https://doi.org/10.1063/1.1728288.

[37] K. N. Tu. "Recent advances on electromigration in very-large-scale-integration of interconnects". In: *Journal of Applied Physics* 94.9 (2003), pp. 5451–5473. eprint: https://doi.org/10.1063/1.1611263.

[38] H.B. Huntington and A.R. Grone. "Current-induced marker motion in gold wires". In: *Journal of Physics and Chemistry of Solids* 20.1 (1961), pp. 76 –87.

[39] I. A. Blech. "Electromigration in thin aluminum films on titanium nitride". In: *Journal of Applied Physics* 47.4 (1976), pp. 1203–1208. eprint: https://doi.org/10.1063/1.322842.

[40] J. R. Black. "Electromigration—A brief survey and some recent results". In: *IEEE Transactions on Electron Devices* 16.4 (1969), pp. 338–347.

[41] J. R. Lloyd. "Electromigration failure". In: *Journal of Applied Physics* 69.11 (1991), pp. 7601–7604. eprint: https://doi.org/10.1063/1.347529.

[42] E. T. Ogawa, Ki-Don Lee, V. A. Blaschke, and P. S. Ho. “Electromigration reliability issues in dual-damascene Cu interconnections”. In: *IEEE Transactions on Reliability* 51.4 (2002), pp. 403–419.

[43] A. H. Fischer, O. Aubel, J. Gill, T. C. Lee, B. Li, C. Christiansen, F. Chen, M. Angyal, T. Bolom, and E. Kaltalioglu. “Reliability Challenges in Copper Metallizations arising with the PVD Resputter Liner Engineering for 65nm and Beyond”. In: *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*. 2007, pp. 511–515.

[44] Baozhen Li, T. D. Sullivan, and T. C. Lee. “Line depletion electromigration characterization of Cu interconnects”. In: *IEEE Transactions on Device and Materials Reliability* 4.1 (2004), pp. 80–85.

[45] E. T. Ogawa, J. W. McPherson, J. A. Rosal, K. J. Dickerson, T. C. Chiu, L. Y. Tsung, M. K. Jain, T. D. Bonifield, J. C. Ondrusek, and W. R. McKee. “Stress-induced voiding under vias connected to wide Cu metal leads”. In: *2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320)*. 2002, pp. 312–321.

[46] J. Klema, R. Pyle, and E. Domangue. “Reliability Implications of Nitrogen Contamination During Deposition of Sputtered Aluminum/Silicon Metal Films”. In: *22nd International Reliability Physics Symposium*. 1984, pp. 1–5.

[47] J. T. Yue, W. P. Funsten, and R. V. Taylor. “Stress Induced Voids in Aluminum Interconnects During IC Processing”. In: *23rd International Reliability Physics Symposium*. 1985, pp. 126–137.

[48] J. W. McPherson and C. F. Dunn. “A model for stress-induced metal notching and voiding in very large-scale-integrated Al–Si (1%) metallization”. In: *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena* 5.5 (1987), pp. 1321–1325. eprint: `https://avs.scitation.org/doi/pdf/10.1116/1.583609`.

[49] K. Y. Y. Doong, R. C. J. Wang, S. C. Lin, L. J. Hung, C. C. Chiu, D. Su, K. Wu, K. L. Young, and Y. K. Peng. “Stress-induced voiding and its geometry dependency characterization”. In: *2003 IEEE International Reliability Physics Symposium Proceedings, 2003. 41st Annual.* 2003, pp. 156–160.

[50] Y. K. Lim, Y. H. Lim, C. S. Seet, B. C. Zhang, K. L. Chok, K. H. See, T. J. Lee, L. C. Hsia, and K. L. Pey. “Stress-induced voiding in multi-level copper/low-k interconnects”. In: *2004 IEEE International Reliability Physics Symposium. Proceedings*. 2004, pp. 240–245.

[51] M. Hommel and S. Penka. “Size Effects and Temperature Dependence of Stress-Induced Voiding”. In: *2006 IEEE International Reliability Physics Symposium Proceedings*. 2006, pp. 685–686.

[52] R. G. Southwick, E. Wu, S. Mehta, and J. H. Stathis. “Time dependent dielectric breakdown of SiN, SiBCN and SiOCN spacer dielectrics”. In: *2017 IEEE International Reliability Physics Symposium (IRPS)*. 2017, DG–1.1–DG–1.5.

[53] S. Cha, C. C. Chen, T. Liu, and L. S. Milor. “Extraction of threshold voltage degradation modeling due to Negative Bias Temperature Instability in circuits with I/O measurements”. In: *2014 IEEE 32nd VLSI Test Symposium (VTS)*. 2014, pp. 1–6.

[54] S. Cha, T. Liu, and L. Milor. “Negative Bias Temperature Instability and Gate Oxide Breakdown Modeling in Circuits With Die-to-Die Calibration Through Power Supply and Ground Signal Measurements”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.8 (2017), pp. 2271–2284.

[55] C. C. Chen, T. Liu, and L. Milor. “System-Level Modeling of Microprocessor Reliability Degradation Due to Bias Temperature Instability and Hot Carrier Injection”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24.8 (2016), pp. 2712–2725.

[56] C. C. Chen, Soonyoung Cha, Taizhi Liu, and L. Milor. “System-level modeling of microprocessor reliability degradation due to BTI and HCI”. In: *2014 IEEE International Reliability Physics Symposium*. 2014, CA.8.1–CA.8.9.

[57] Taizhi Liu, Chang-Chih Chen, Soonyoung Cha, and Linda Milor. “System-level variation-aware aging simulator using a unified novel gate-delay model for bias temperature instability, hot carrier injection, and gate oxide breakdown”. In: *Microelectronics Reliability* 55.9 (2015). Proceedings of the 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, pp. 1334 –1340.

[58] E. Maricau and G. Gielen. “Efficient Variability-Aware NBTI and Hot Carrier Circuit Reliability Analysis”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 29.12 (2010), pp. 1884–1893.

[59] R. Zhang, T. Liu, K. Yang, and L. Milor. “Modeling of the reliability degradation of a FinFET-based SRAM due to bias temperature instability, hot carrier injection, and gate oxide breakdown”. In: *2017 IEEE International Integrated Reliability Workshop (IIRW)*. 2017, pp. 1–4.

[60] J. Fang and S. S. Sapatnekar. “The Impact of BTI Variations on Timing in Digital Logic Circuits”. In: *IEEE Transactions on Device and Materials Reliability* 13.1 (2013), pp. 277–286.

[61] D. S. Ang, Z. Q. Teo, T. J. J. Ho, and C. M. Ng. “Reassessing the Mechanisms of Negative-Bias Temperature Instability by Repetitive Stress/Relaxation Experiments”. In: *IEEE Transactions on Device and Materials Reliability* 11.1 (2011), pp. 19–34.

[62] T. Liu, C. C. Chen, and L. Milor. “Comprehensive Reliability-Aware Statistical Timing Analysis Using a Unified Gate-Delay Model for Microprocessors”. In: *IEEE Transactions on Emerging Topics in Computing* 6.2 (2018), pp. 219–232.

[63] J. Fang and S. S. Sapatnekar. “Incorporating Hot-Carrier Injection Effects Into Timing Analysis for Large Circuits”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22.12 (2014), pp. 2738–2751.

[64] B. P. Linder, J. H. Stathis, R. A. Wachnik, E. Wu, S. A. Cohen, A. Ray, and A. Vayshenker. “Gate oxide breakdown under Current Limited Constant Voltage Stress”. In: *2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104)*. 2000, pp. 214–215.

[65] R. Rodriguez, J. H. Stathis, B. P. Linder, S. Kowalczyk, C. T. Chuang, R. V. Joshi, G. Northrop, K. Bernstein, A. J. Bhavnagarwala, and S. Lombardo. “The impact of gate-oxide breakdown on SRAM stability”. In: *IEEE Electron Device Letters* 23.9 (2002), pp. 559–561.

[66] R. Rodriguez, J. H. Stathis, and B. P. Linder. “A model for gate-oxide breakdown in CMOS inverters”. In: *IEEE Electron Device Letters* 24.2 (2003), pp. 114–116.

[67] Dae-Hyun Kim and Linda Milor. “Analysis of errors in estimating wearout characteristics of time-dependent dielectric breakdown using system-level accelerated life test”. In: *Microelectronics Reliability* 76-77 (2017), pp. 47 –52.

[68] D. Kim and L. Milor. “A methodology for estimating memory lifetime using a system-level accelerated life test and error-correcting codes”. In: *2017 IEEE 35th VLSI Test Symposium (VTS)*. 2017, pp. 1–6.

[69] K. Yang, T. Liu, R. Zhang, and L. Milor. “A Comprehensive Time-Dependent Dielectric Breakdown Lifetime Simulator for Both Traditional CMOS and FinFET Technology”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 26.11 (2018), pp. 2470–2482.

[70] M. Bashir, D. H. Kim, K. Athikulwongse, S. K. Lim, and L. Milor. “Backend low-k TDDB chip reliability simulator”. In: *2011 International Reliability Physics Symposium*. 2011, pp. 2C.2.1–2C.2.10.

[71] Muhammad Bashir and Linda Milor. “Towards a Chip Level Reliability Simulator for Copper/Low-k Backend Processes”. In: *Proceedings of the Conference on*

Design, Automation and Test in Europe. DATE '10. Dresden, Germany: European Design and Automation Association, 2010, pp. 279–282. ISBN: 978-3-9810801-6-2.

[72] Muhammad Bashir, Linda Milor, Dae Hyun Kim, and Sung Kyu Lim. "Methodology to determine the impact of linewidth variation on chip scale copper/low-k backend dielectric breakdown". In: *Microelectronics Reliability* 50.9 (2010). 21st European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis, pp. 1341 –1346.

[73] M. M. Bashir and L. Milor. "Impact of Linewidth on Backend Dielectric TDDB and Incorporation of the Linewidth Effect in Full Chip Lifetime Analysis". In: *IEEE Transactions on Semiconductor Manufacturing* 28.1 (2015), pp. 25–34.

[74] Chang-Chih Chen and Linda Milor. "System-level Modeling and Microprocessor Reliability Analysis for Backend Wearout Mechanisms". In: *Proceedings of the Conference on Design, Automation and Test in Europe*. DATE '13. Grenoble, France: EDA Consortium, 2013, pp. 1615–1620. ISBN: 978-1-4503-2153-2.

[75] Feifei He and Cher Ming Tan. "Electromigration reliability of interconnections in RF low noise amplifier circuit". In: *Microelectronics Reliability* 52.2 (2012). Low Temperature Processing for Microelectronics and Microsystems Packaging, pp. 446 –454.

[76] X. Huang, A. Kteyan, S. X. D. Tan, and V. Sukharev. "Physics-Based Electromigration Models and Full-Chip Assessment for Power Grid Networks". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 35.11 (2016), pp. 1848–1861.

[77] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim. "TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 31.8 (2012), pp. 1194–1207.

[78] C. Jiang, T. G. Habetler, and W. Cao. "Improved condition monitoring of the faulty blower wheel driven by brushless DC motor in air handler unit (AHU)". In: *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2016, pp. 1–5.

[79] Chen Jiang. "Condition monitoring of high efficiency heating, ventilation and air conditioning systems". PhD thesis. Georgia Institute of Technology, 2017.

[80] K. J. Kuhn. "Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS". In: *2007 IEEE International Electron Devices Meeting*. 2007, pp. 471–474.

[81] D. H. Kim and L. Milor. “Memory reliability estimation degraded by TDDB using circuit-level accelerated life test”. In: *2017 IEEE International Reliability Physics Symposium (IRPS)*. 2017, RT–1.1–RT–1.6.

[82] A. P. Chandrakasan and R. W. Brodersen. “Minimizing power consumption in digital CMOS circuits”. In: *Proceedings of the IEEE* 83.4 (1995), pp. 498–523.

[83] C. Nagendra, M. J. Irwin, and R. M. Owens. “Area-time-power tradeoffs in parallel adders”. In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 43.10 (1996), pp. 689–702.

[84] S. C. Prasad and K. Roy. “Circuit optimization for minimisation of power consumption under delay constraint”. In: *Proceedings of the 8th International Conference on VLSI Design*. 1995, pp. 305–309.

[85] G. Gielen, H. Walscharts, and W. Sansen. “Analog Circuit Design Optimization based on Symbolic Simulation and Simulated Annealing”. In: *Solid-State Circuits Conference, 1989. ESSCIRC ’89. Proceedings of the 15th European*. 1989, pp. 252–255.

[86] K. Antreich, J. Eckmueller, H. Graeb, M. Pronath, F. Schenkel, R. Schwencker, and S. Zizala. “WiCkeD: analog circuit synthesis incorporating mismatch”. In: *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044)*. 2000, pp. 511–514.

[87] Rui Zhang, Taizhi Liu, Kexin Yang, and Linda Milor. “Analysis of time-dependent dielectric breakdown induced aging of SRAM cache with different configurations”. In: *Microelectronics Reliability* 76-77 (2017), pp. 87 –91.

[88] K. Yang and L. Milor. “Impact of stress acceleration on mixed-signal gate oxide lifetime”. In: *2015 IEEE 20th International Mixed-Signals Testing Workshop (IMSTW)*. 2015, pp. 1–6.

[89] K. Yang, T. Liu, R. Zhang, and L. Milor. “Circuit-level reliability simulator for front-end-of-line and middle-of-line time-dependent dielectric breakdown in FinFET technology”. In: *2018 IEEE 36th VLSI Test Symposium (VTS)*. 2018, pp. 1–6.

[90] K. Yang, T. Liu, R. Zhang, and L. Milor. “A comparison study of time-dependent dielectric breakdown for analog and digital circuit’s optimal accelerated test regions”. In: *2017 32nd Conference on Design of Circuits and Integrated Systems (DCIS)*. 2017, pp. 1–6.

[91] Kexin Yang, Taizhi Liu, Rui Zhang, Dae-Hyun Kim, and Linda Milor. "Front-end of line and middle-of-line time-dependent dielectric breakdown reliability simulator for logic circuits". In: *Microelectronics Reliability* 76-77 (2017), pp. 81 –86.

[92] X. Li, J. Qin, and J. B. Bernstein. "Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation". In: *IEEE Transactions on Device and Materials Reliability* 8.1 (2008), pp. 98–121.

[93] J. G. Ahn, M. F. Lu, N. Navale, D. Graves, G. Refai-Ahmed, P. C. Yeh, and J. Chang. "Product-level reliability estimator with budget-based reliability management in 16nm technology". In: *2017 IEEE International Reliability Physics Symposium (IRPS)*. 2017, 3A–3.1–3A–3.6.

[94] K. Y. Yiang, H. W. Yao, and A. Marathe. "TDDB Kinetics and their Relationship with the E- and square root of E-models". In: *2008 International Interconnect Technology Conference*. 2008, pp. 168–170.

[95] Ji-Woon Yang and J. G. Fossum. "On the feasibility of nanoscale triple-gate CMOS transistors". In: *IEEE Transactions on Electron Devices* 52.6 (2005), pp. 1159–1164.

[96] Mayler Martins, Jody Maick Matos, Renato P. Ribas, André Reis, Guilherme Schlinker, Lucio Rech, and Jens Michelsen. "Open Cell Library in 15Nm FreePDK Technology". In: *Proceedings of the 2015 Symposium on International Symposium on Physical Design*. ISPD '15. Monterey, California, USA: ACM, 2015, pp. 171–178. ISBN: 978-1-4503-3399-3.

[97] Rafael J. Segura and Francisco R. Feito. "An algorithm for determining intersection segment-polygon in 3D". In: *Computers & Graphics* 22.5 (1998), pp. 587 –592.

[98] Kirti Bhanushali and W. Rhett Davis. "FreePDK15: An Open-Source Predictive Process Design Kit for 15Nm FinFET Technology". In: *Proceedings of the 2015 Symposium on International Symposium on Physical Design*. ISPD '15. Monterey, California, USA: ACM, 2015, pp. 165–170. ISBN: 978-1-4503-3399-3.

[99] Synopsys Inc. *Design Compiler [Software]*. Available at `https://www.synopsys.com/support/training/rtl-synthesis/design-compiler-rtl-synthesis.html`.

[100] Synopsys Inc. *PrimeTime [Software]*. Available at `https://www.synopsys.com/implementation-and-signoff/signoff/primetime.html`.

[101] COMSOL Inc. *COMSOL*. Available at `https://www.comsol.com/`.

[102] R. Kwasnick, A. E. Papathanasiou, M. Reilly, A. Rashid, B. Zaknoon, and J. Falk. "Determination of CPU use conditions". In: *2011 International Reliability Physics Symposium*. 2011, pp. 2C.3.1–2C.3.6.

[103] M. R. Guthaus, J. S. Ringenberg, D. Ernst, T. M. Austin, T. Mudge, and R. B. Brown. "MiBench: A free, commercially representative embedded benchmark suite". In: *Proceedings of the Fourth Annual IEEE International Workshop on Workload Characterization. WWC-4 (Cat. No.01EX538)*. 2001, pp. 3–14.

[104] J. Jacquelin. "Inference of sampling on Weibull parameter estimation". In: *IEEE Transactions on Dielectrics and Electrical Insulation* 3.6 (1996), pp. 809–816.

[105] Gints Jekabsons. "ARESLab: Adaptive regression splines toolbox for Matlab/Octave". In: *URL: http://www. cs. rtu. lv/jekabsons* (2011).

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